LABORATÓRIO DE LÓGICA CONFIGURÁVEL

Introdução ao Software Quartus Prime

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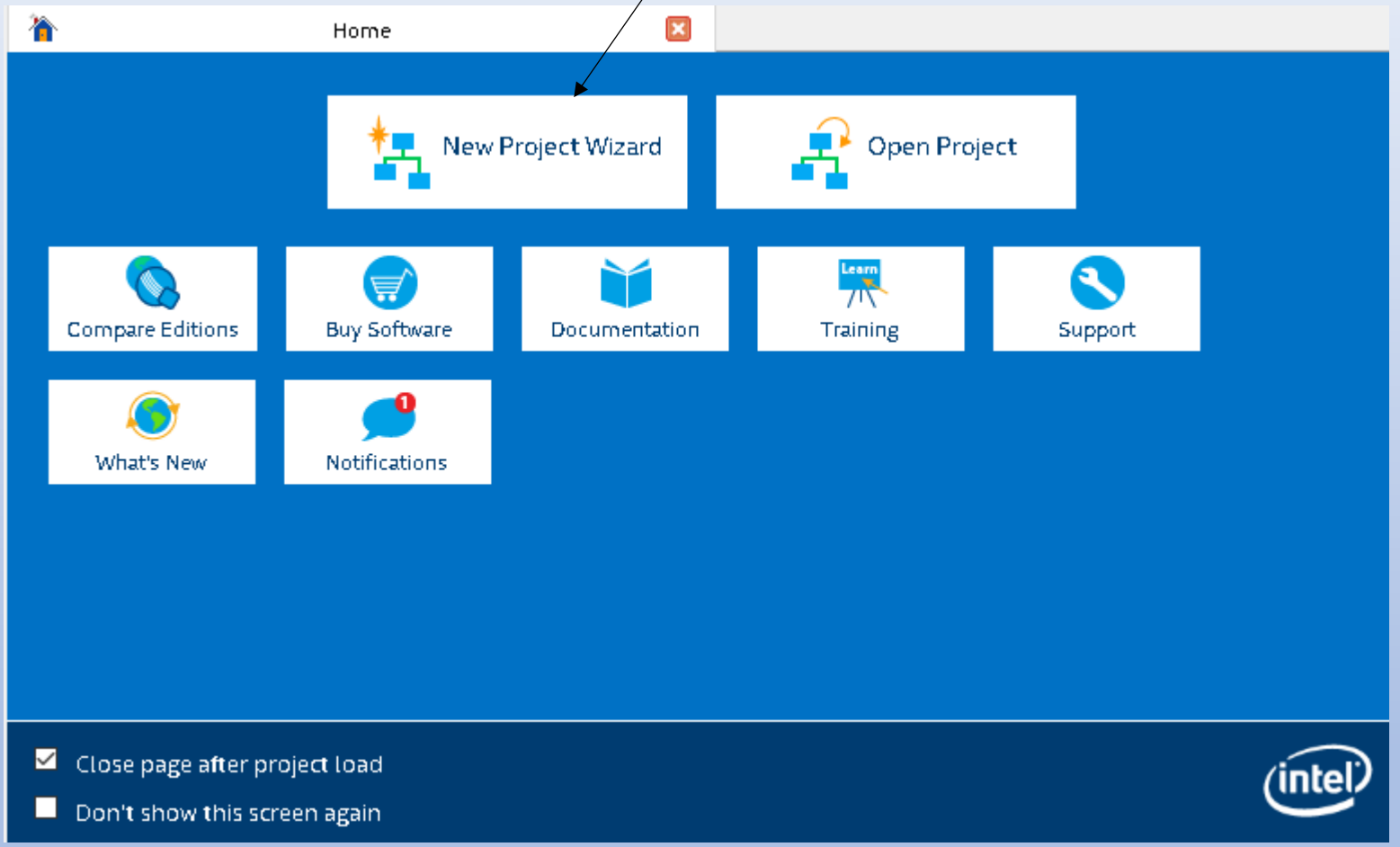
File – New Project Wizard



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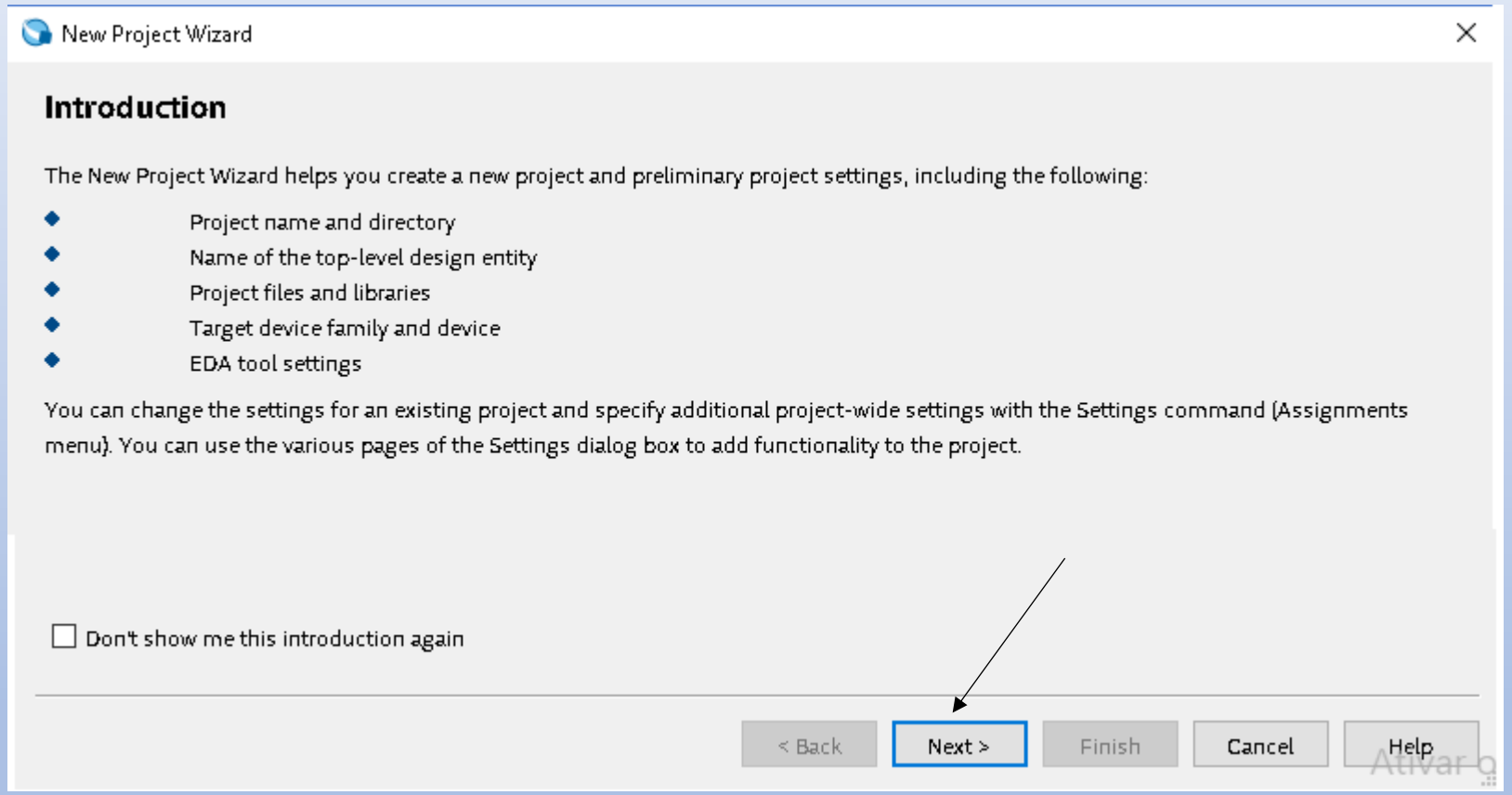
1. New Project ou Create a New Project

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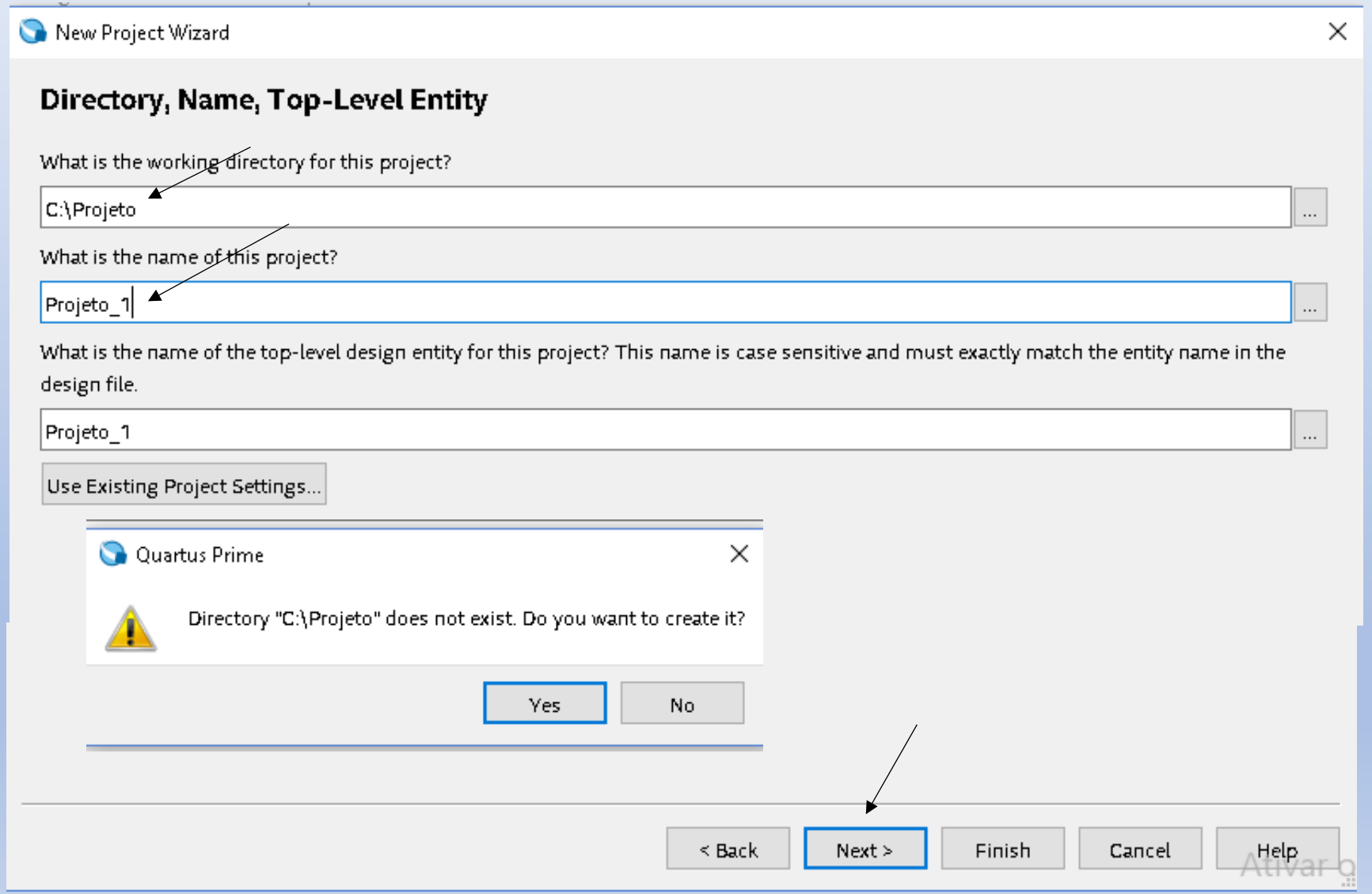
Criar o diretorio: Projeto e Nome do Projeto: Projeto_1



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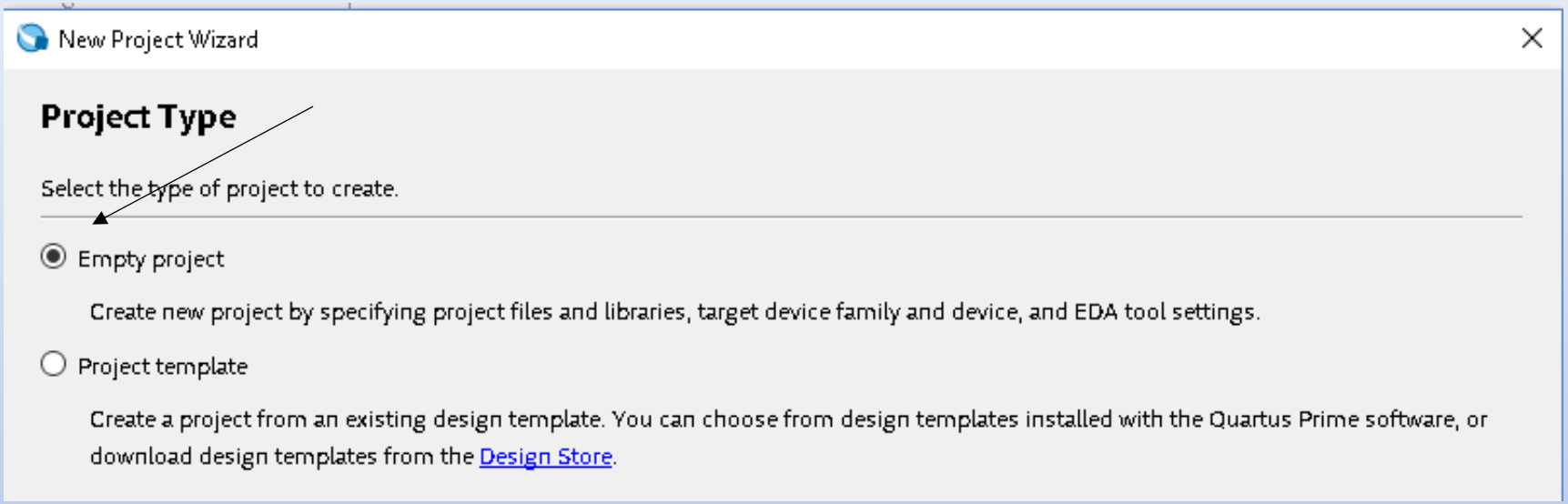

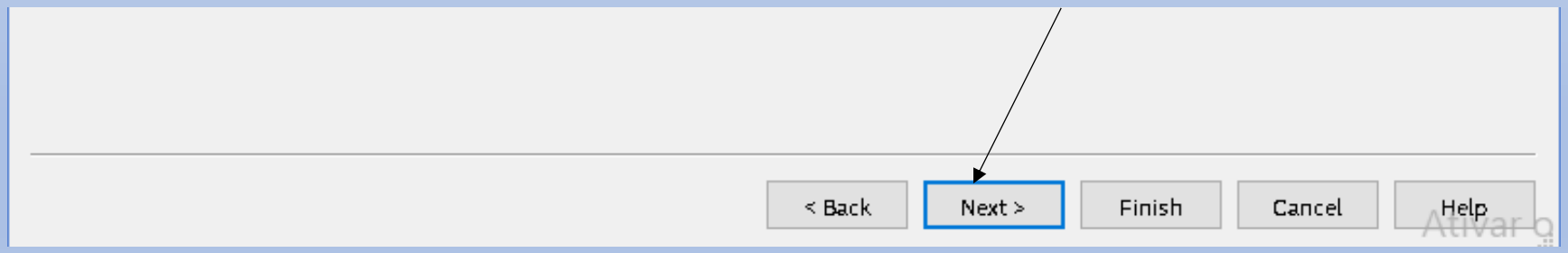

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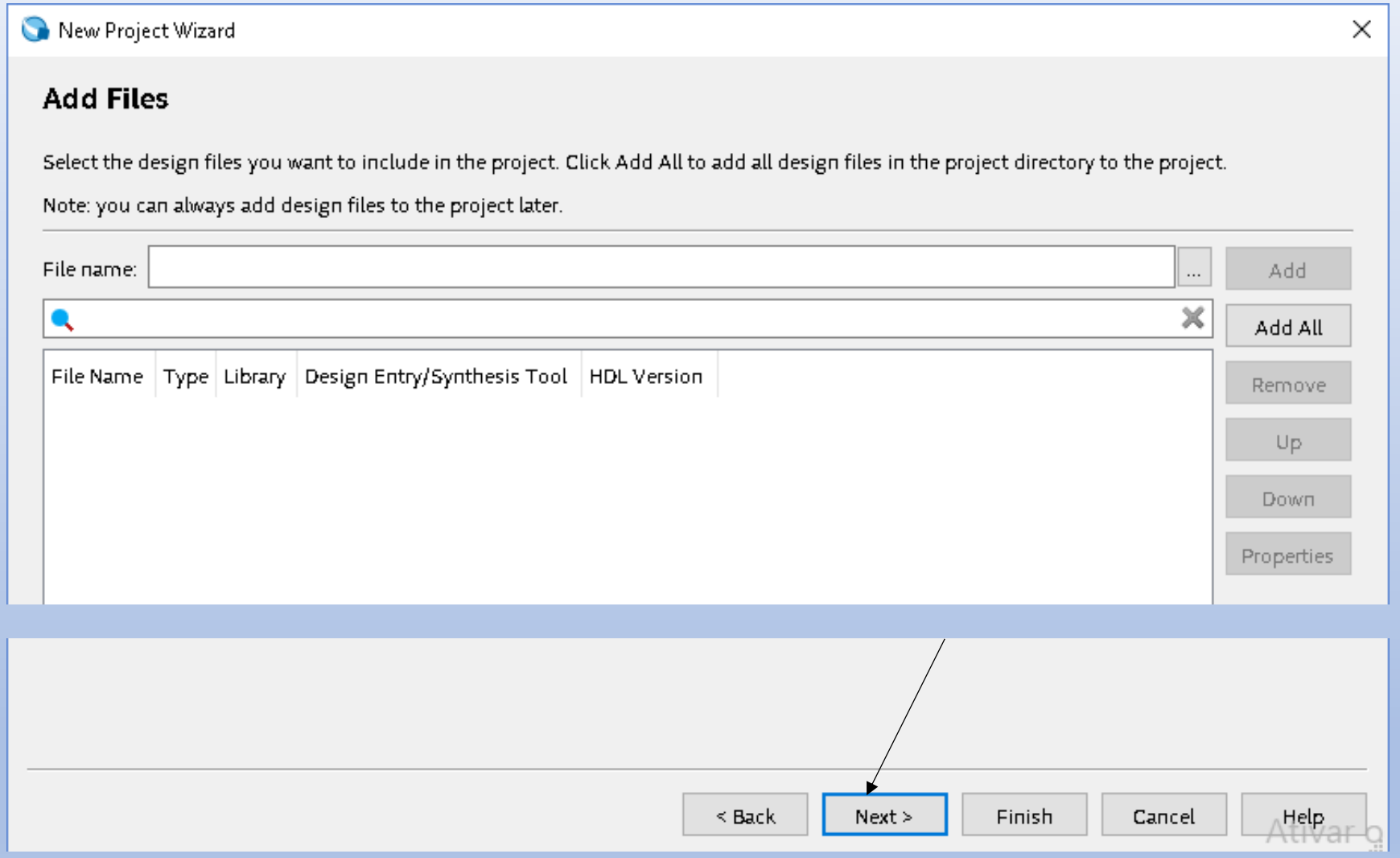

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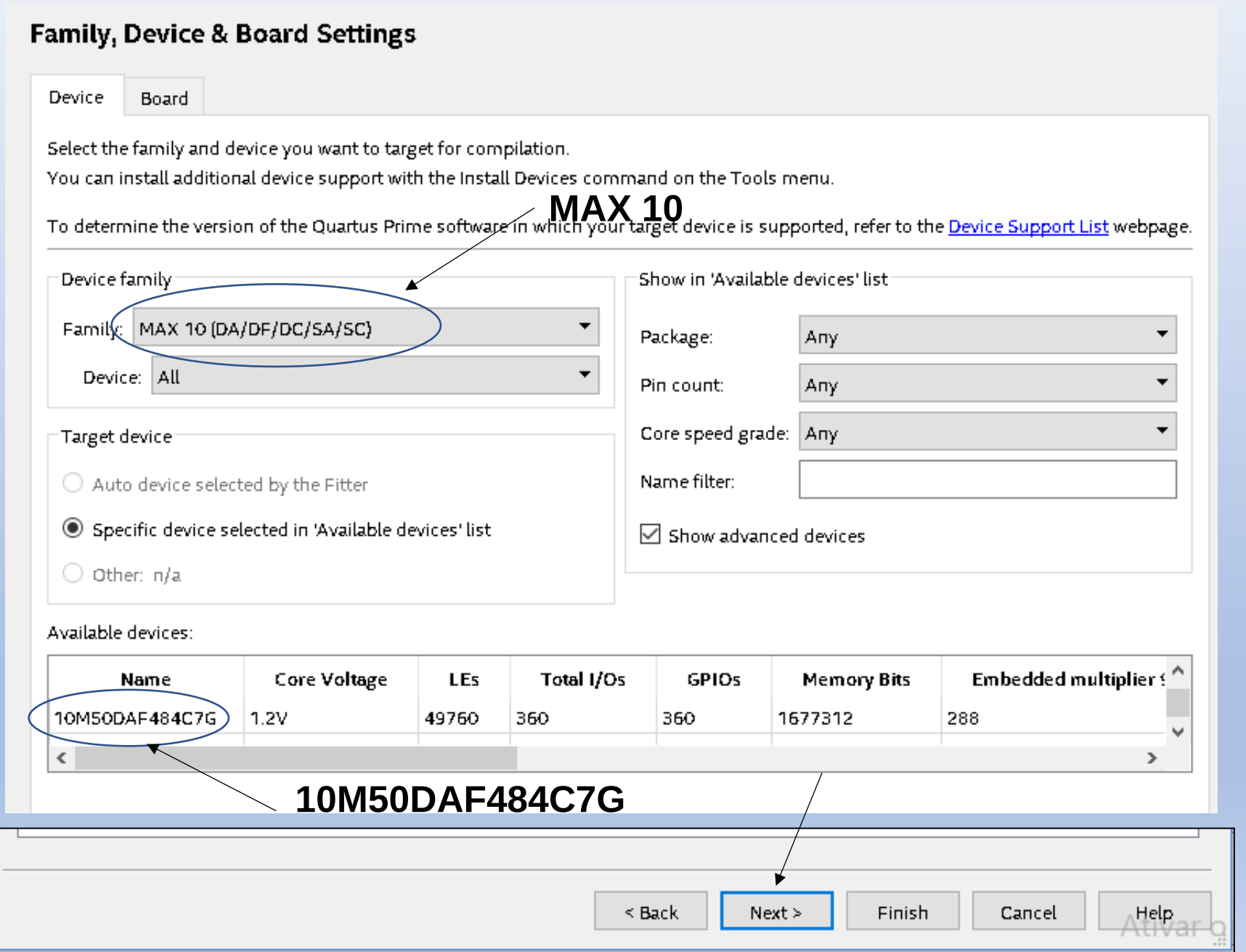

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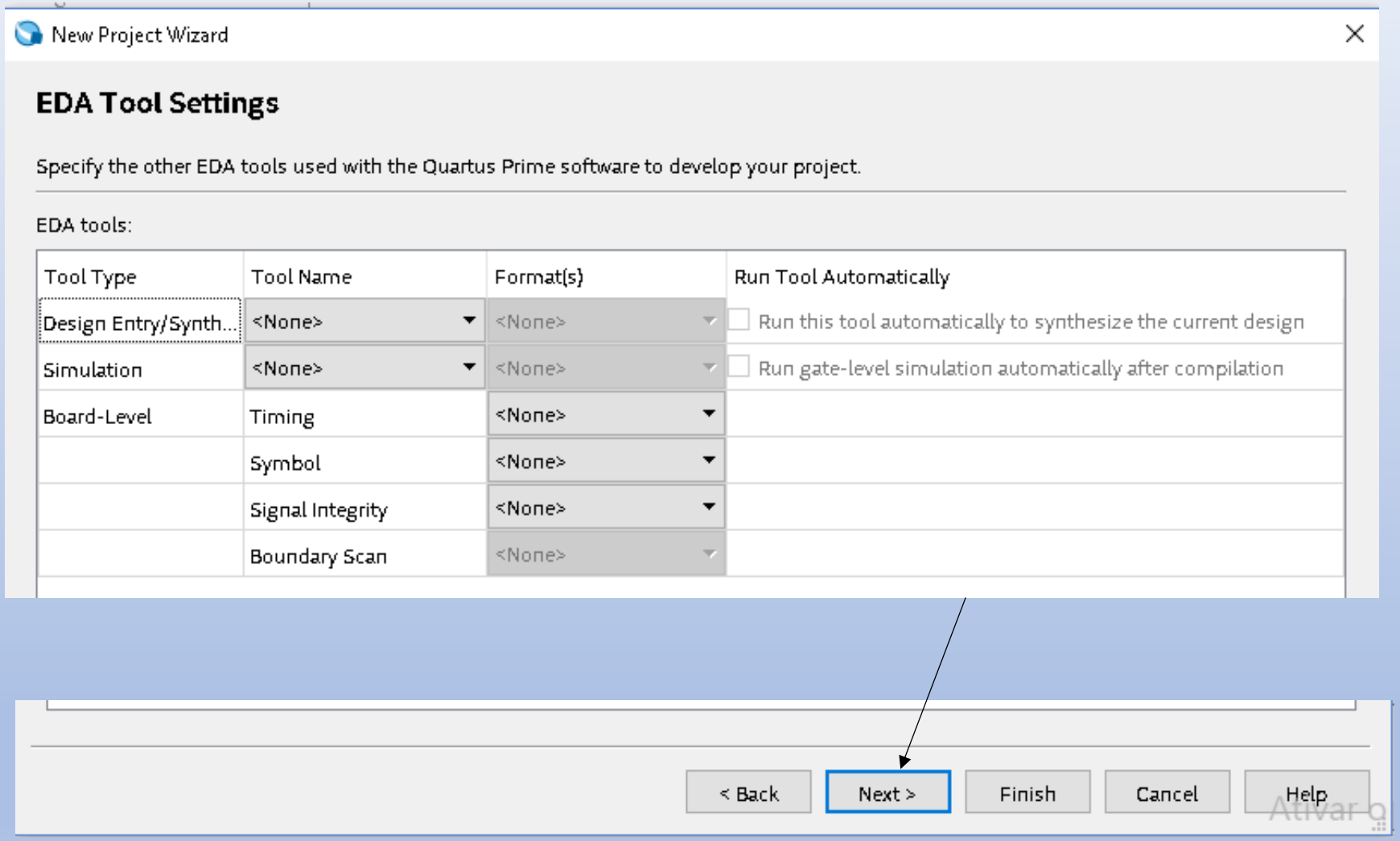

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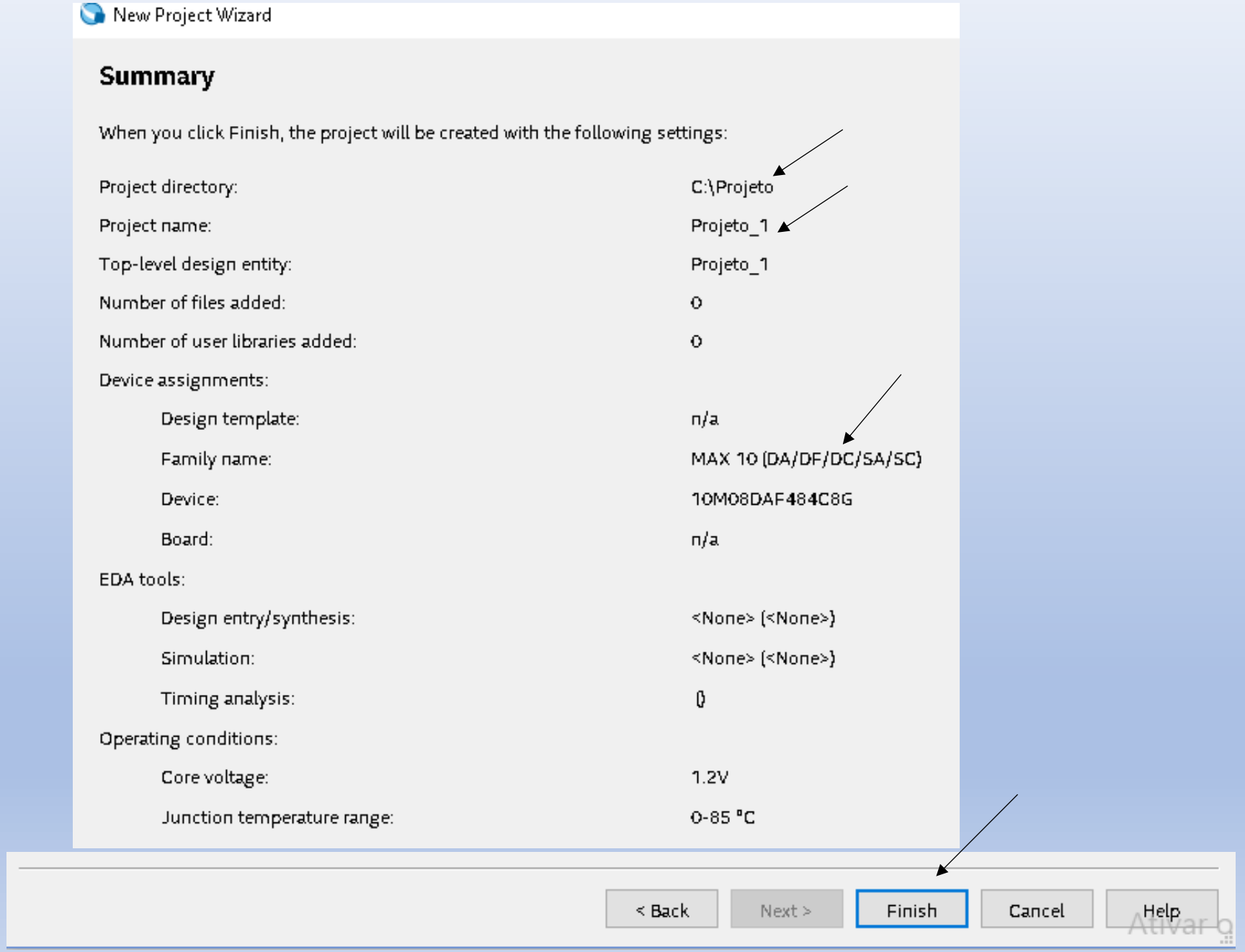

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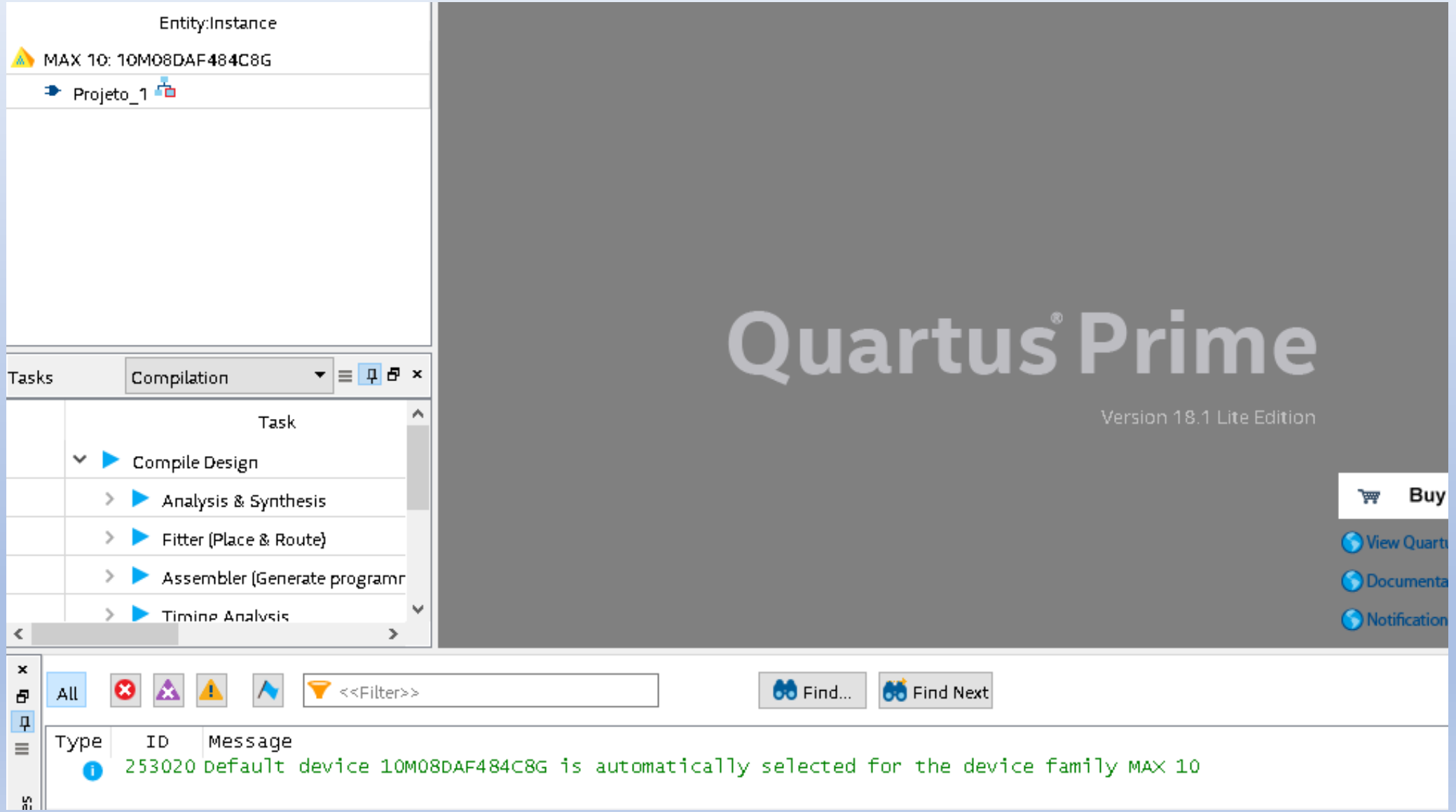
A tela indica que o projeto foi criado.



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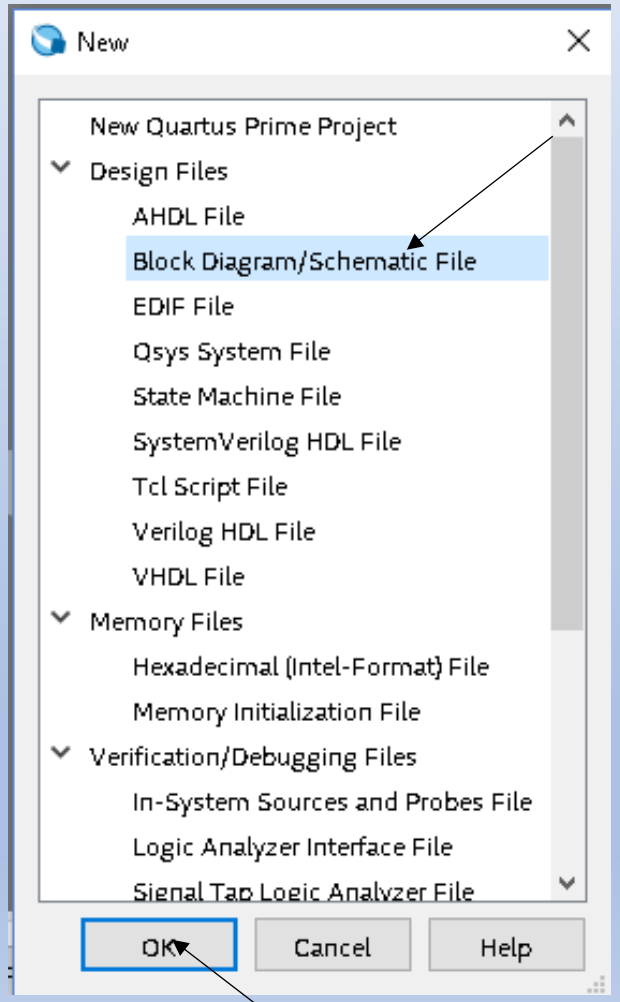
File – New – Block Diagram/Schematic File



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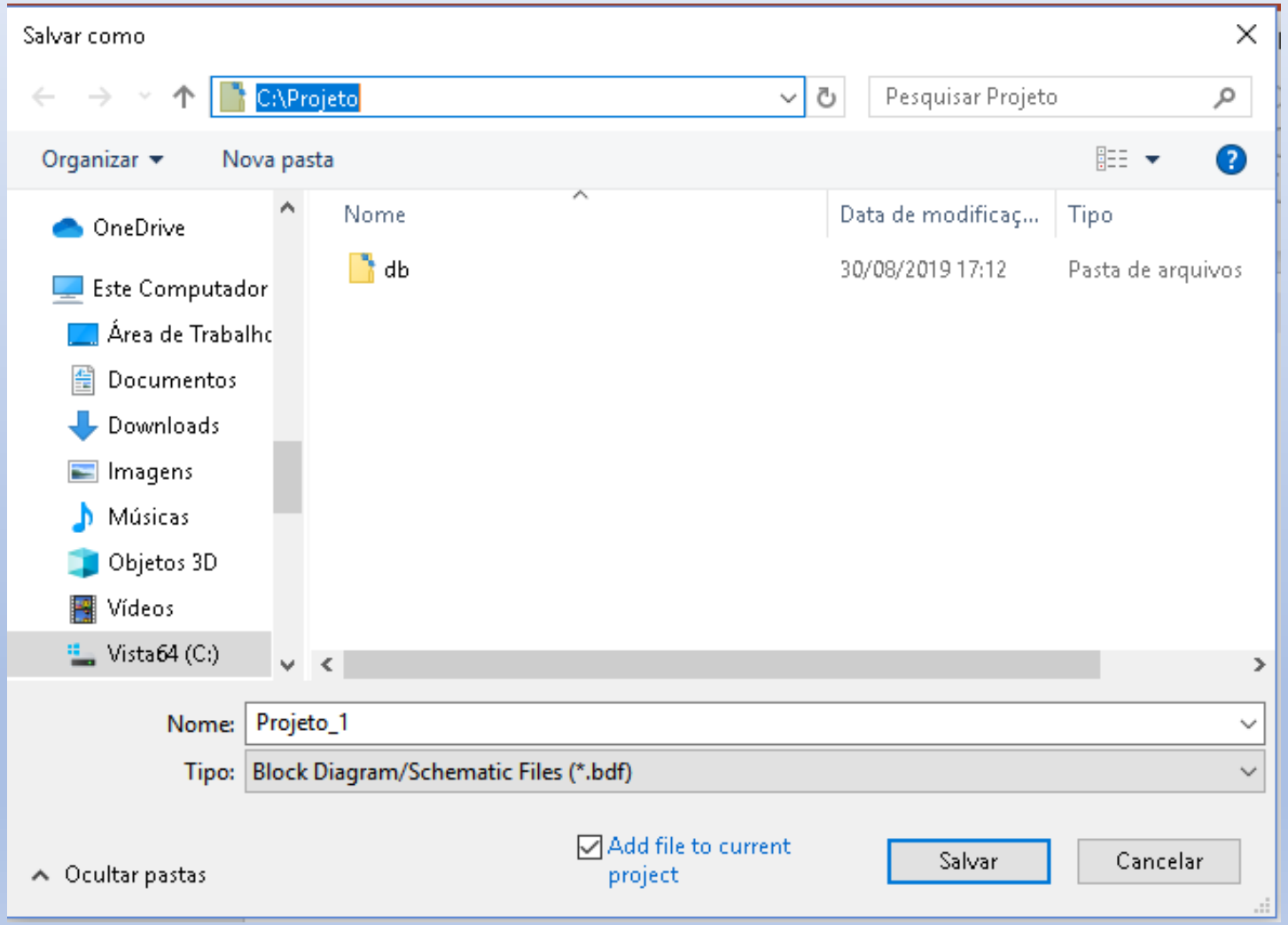
Editor Grafico

File – Save As – Projeto_1 (Pasta Projeto)



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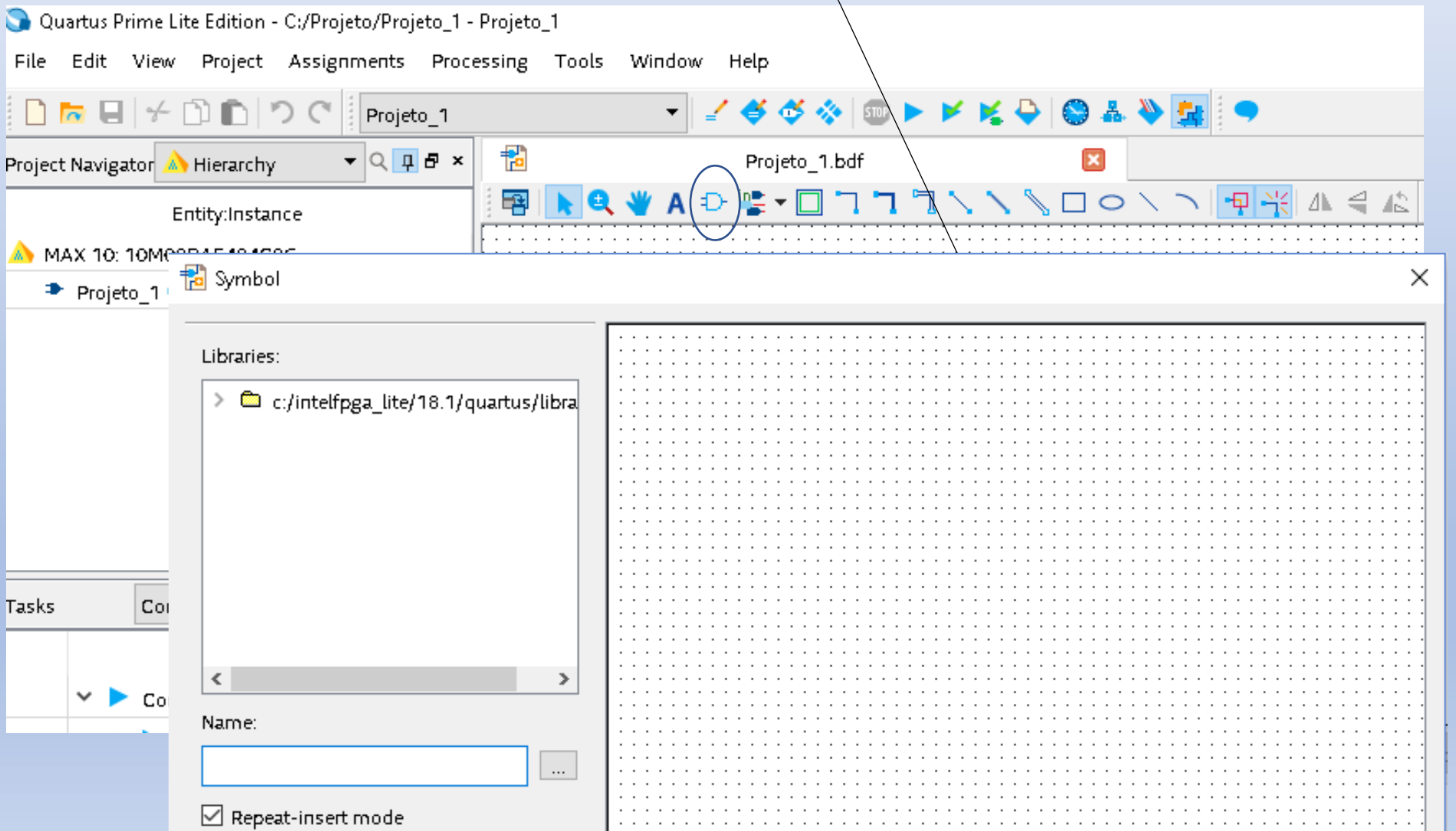
Editor Grafico

- 2 clicks no meio da tela de trabalho surge a tela symbol



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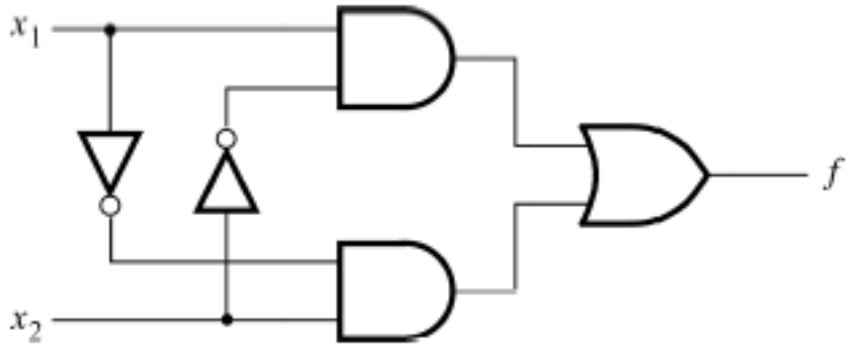
Exercicio 1:



x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	0

Figure 12. The light controller circuit.

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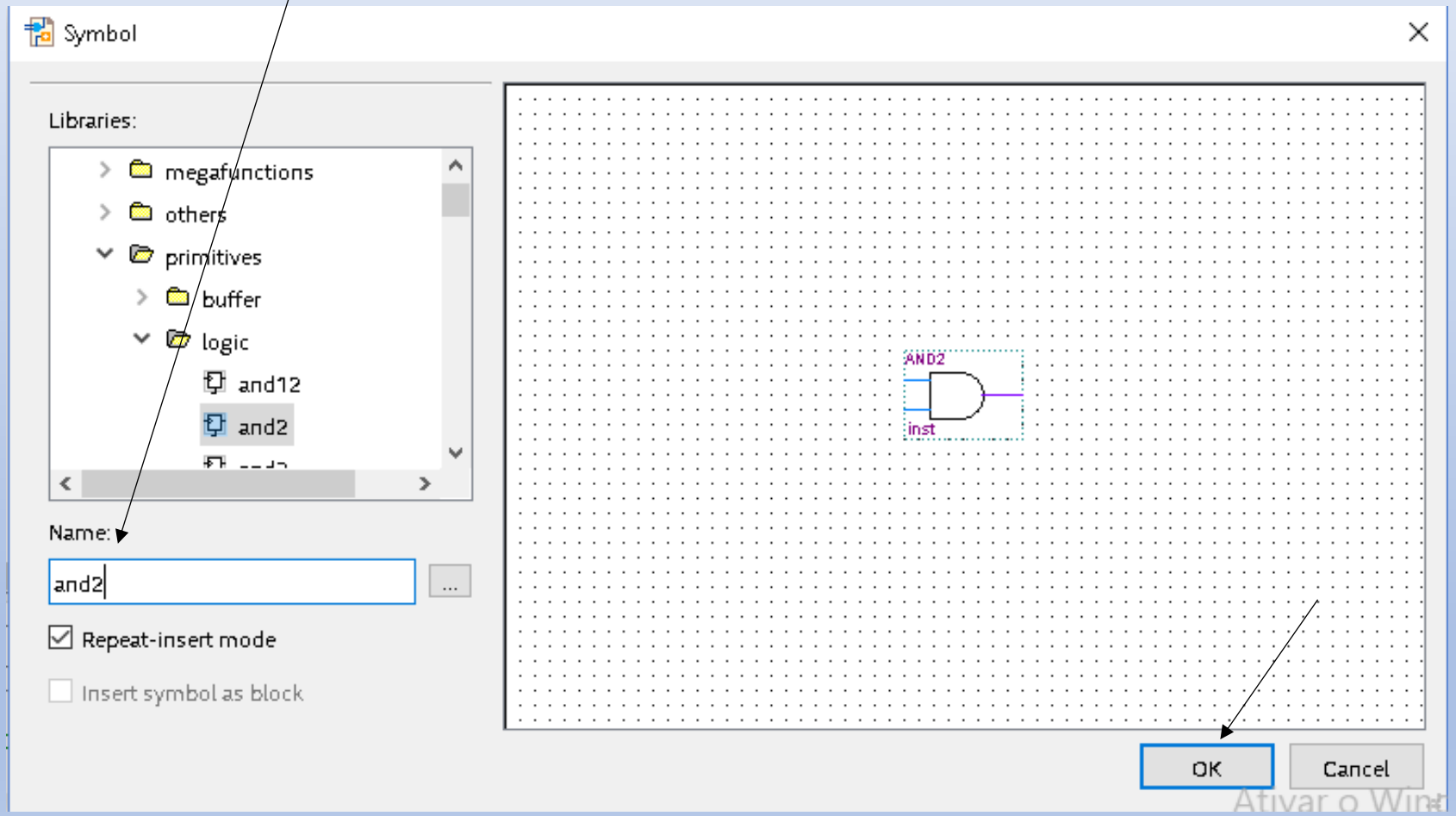
Inserir os componentes desejados



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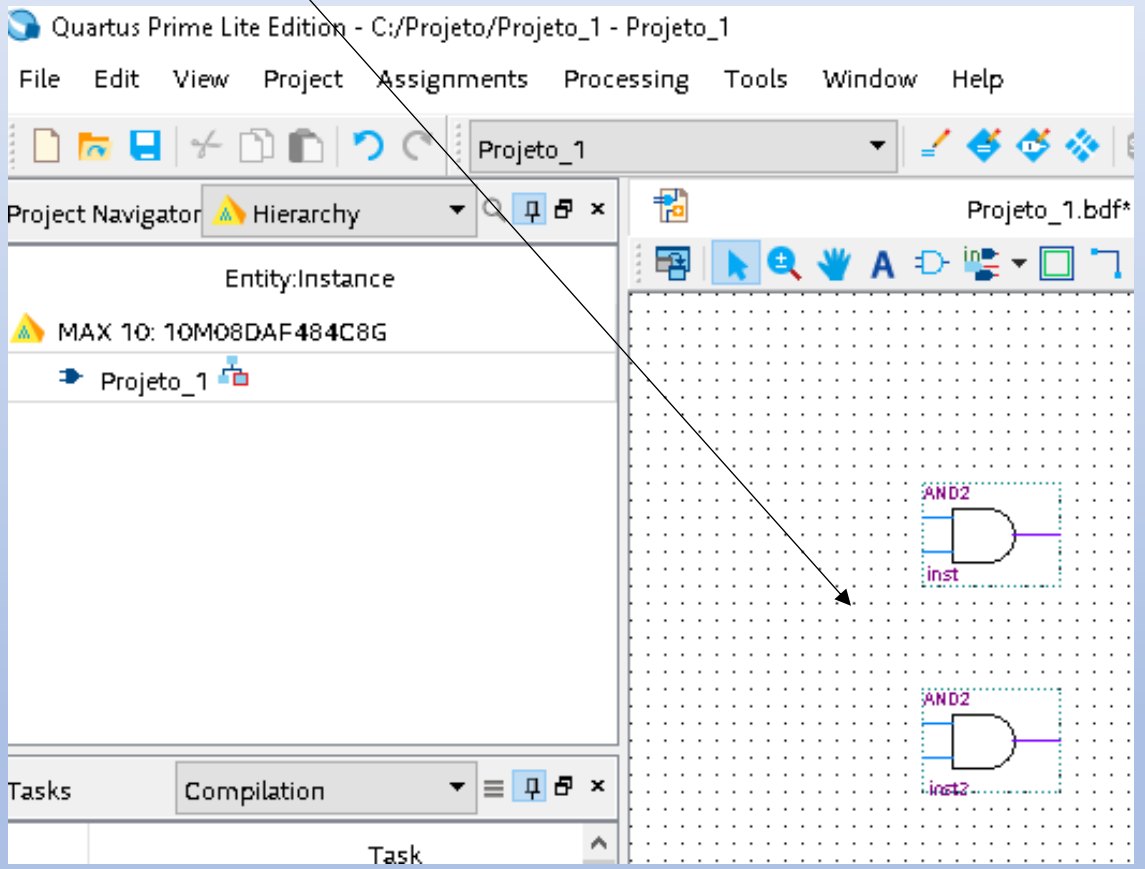
Inserir 2 portas AND



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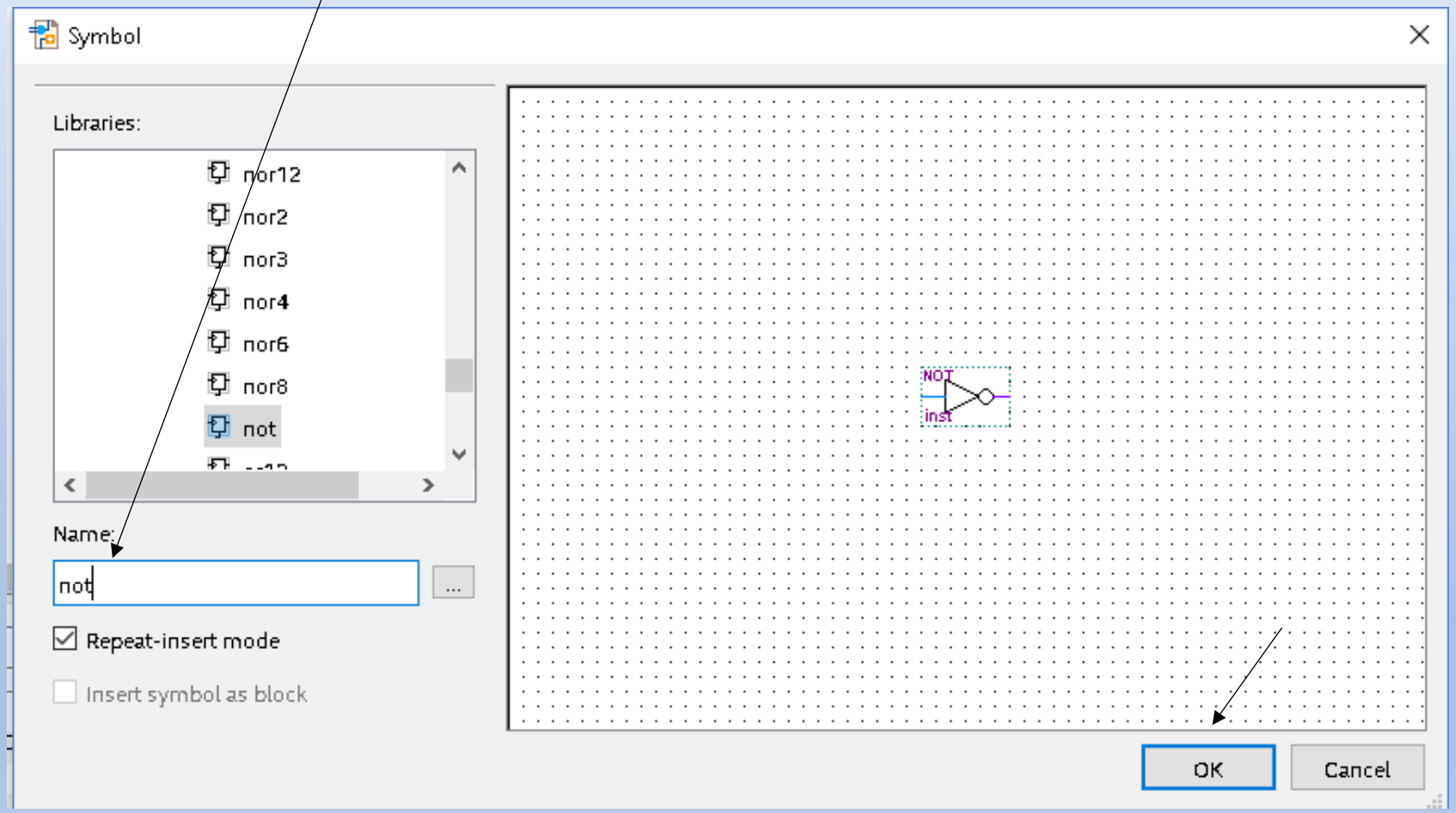
Selecione a porta NOT



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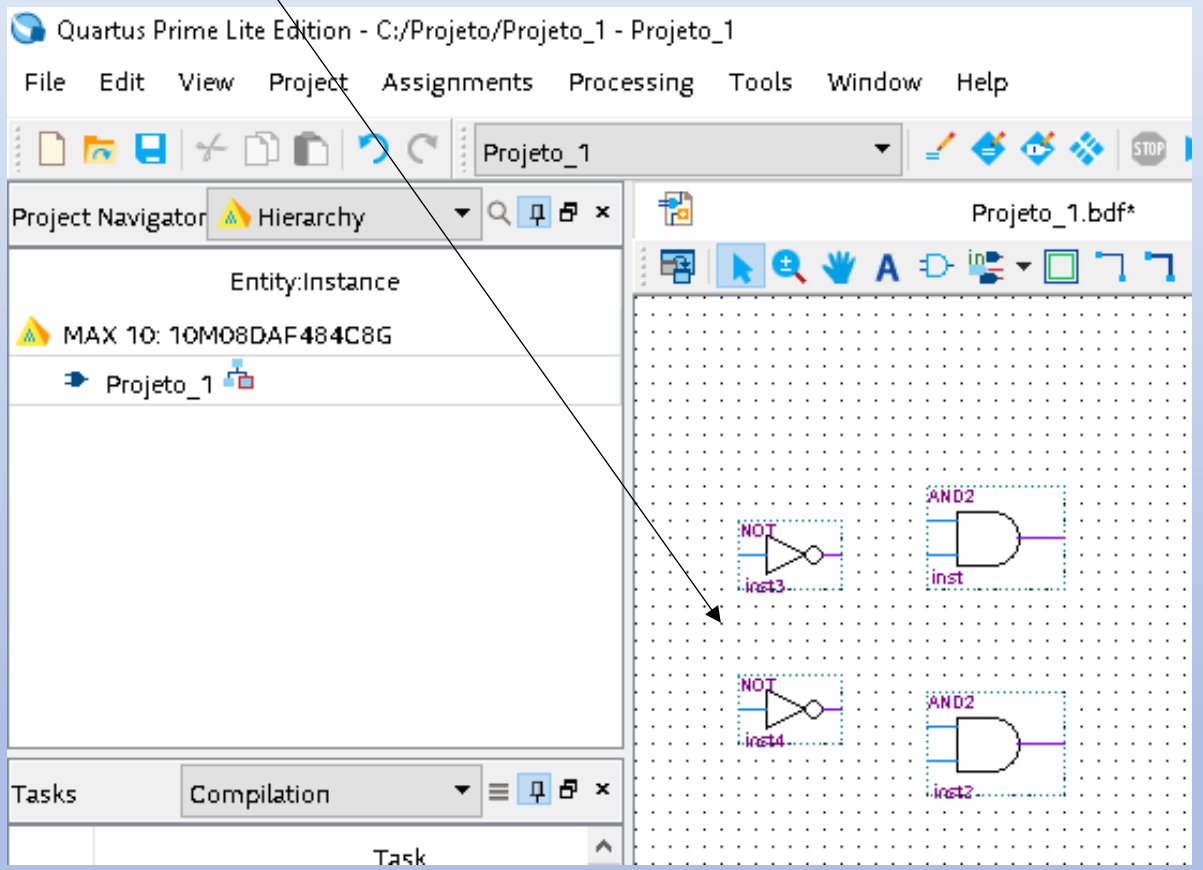
Posicione as duas portas NOT



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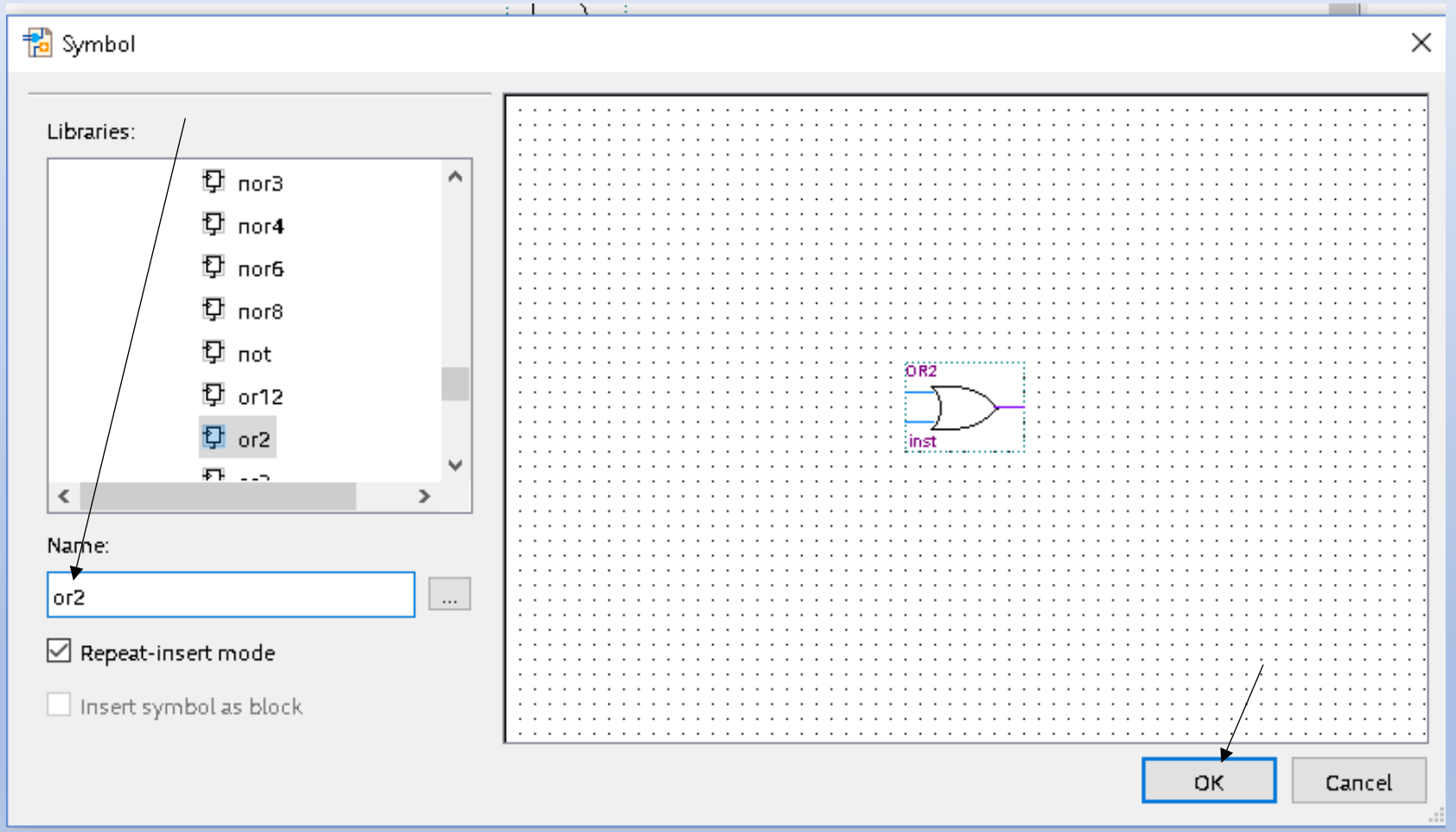
Selecione a porta OR



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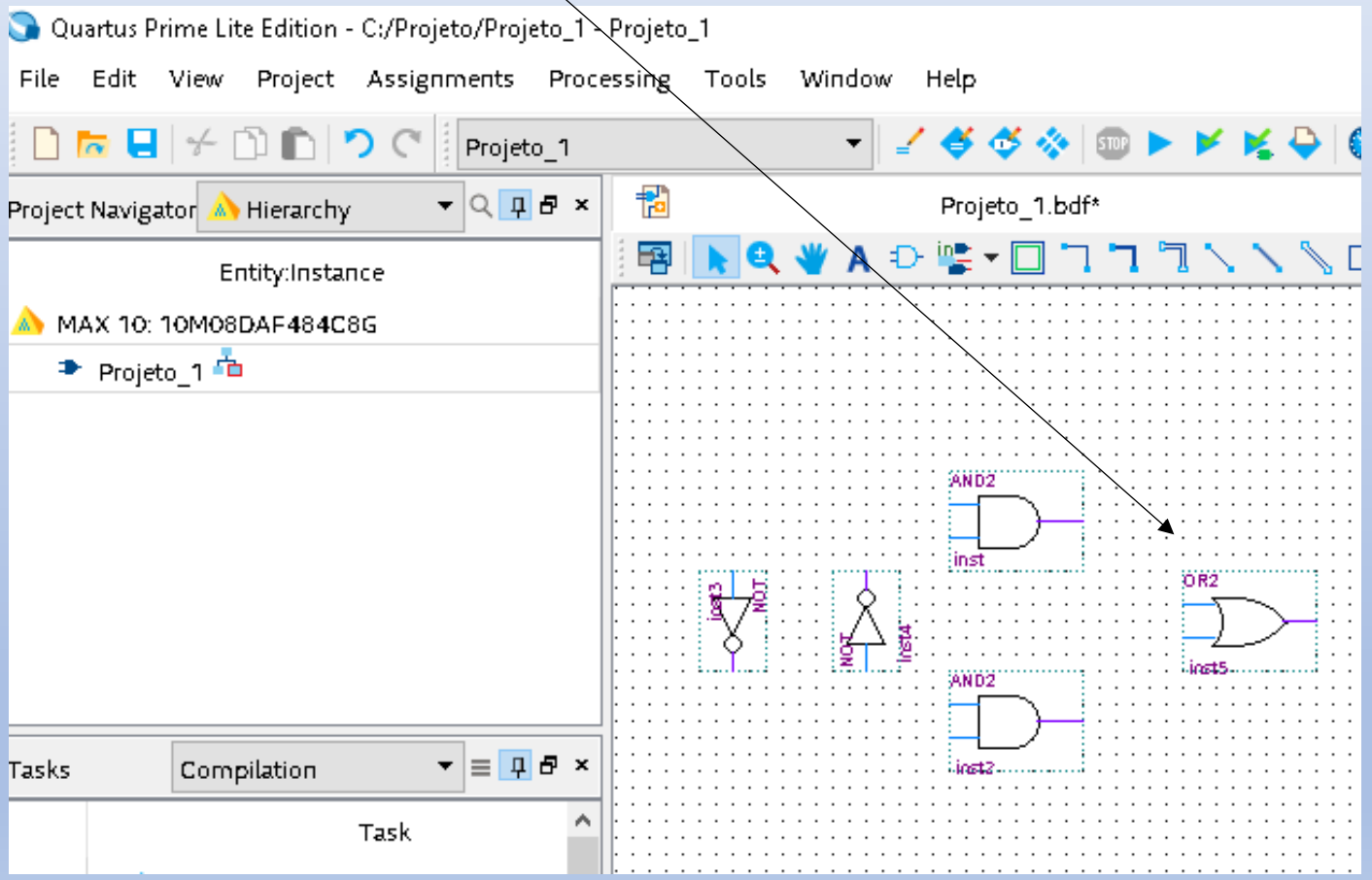
Posicione a porta OR



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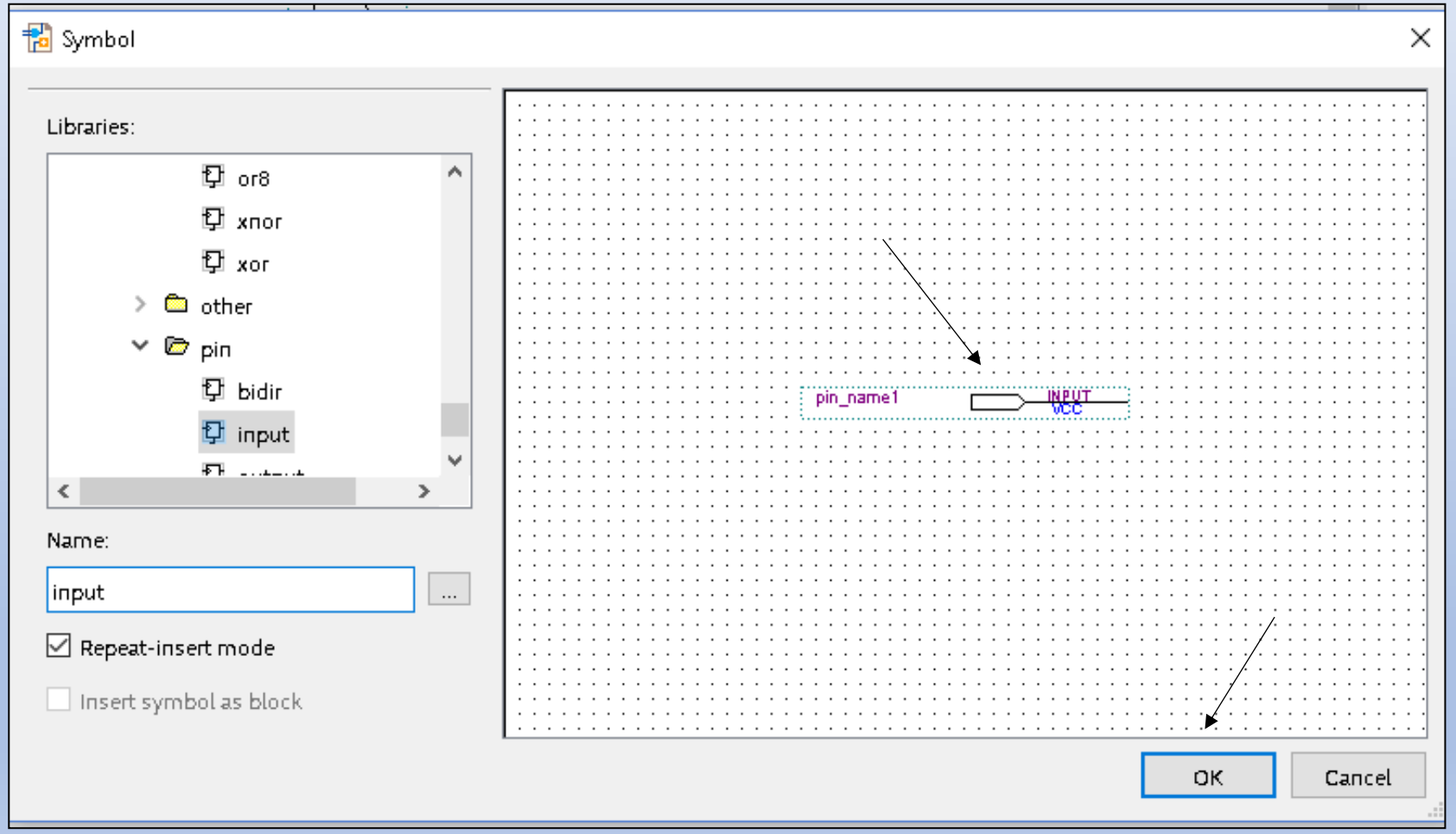
Inserir terminais de entrada



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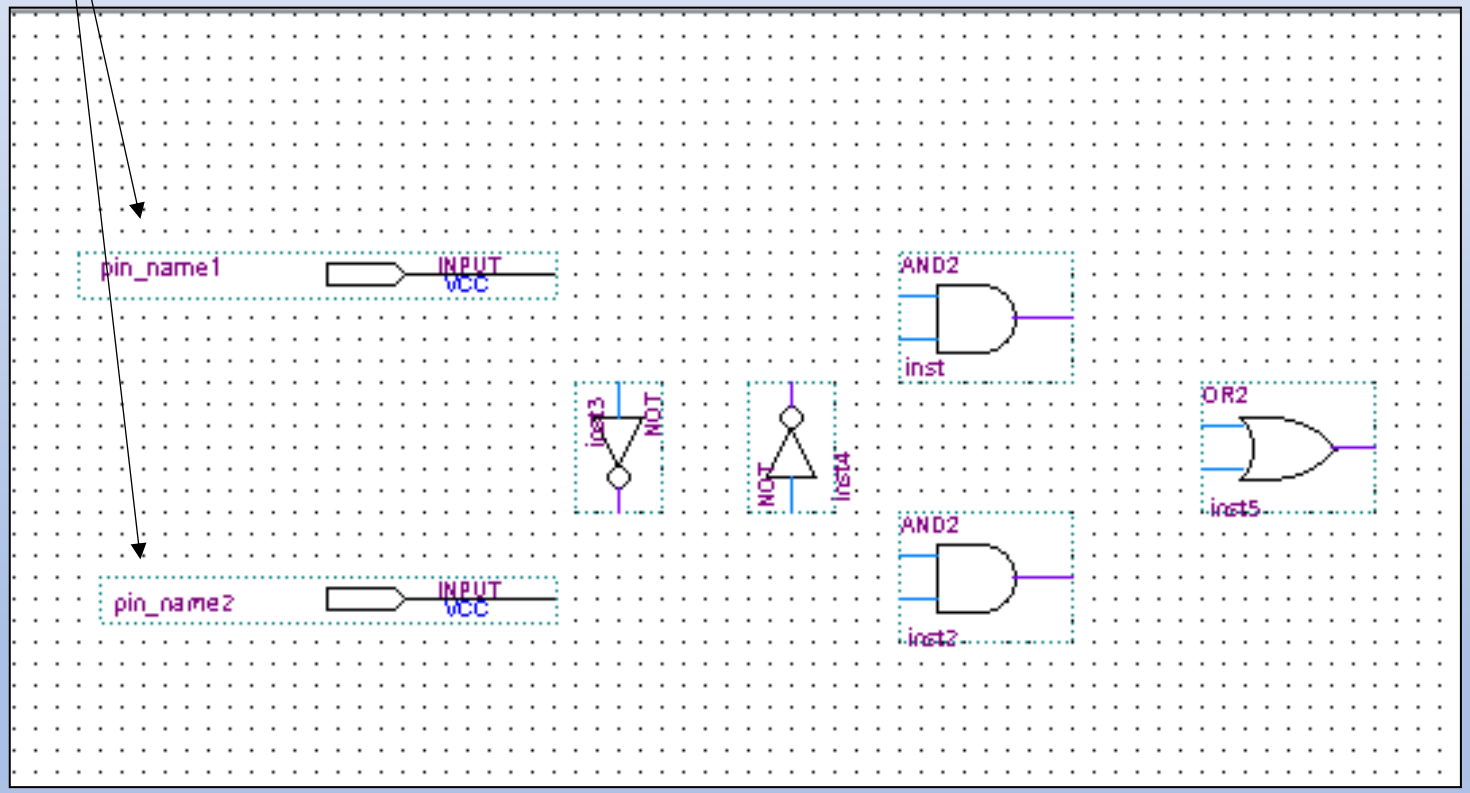
Posicione os 2 terminais de entrada



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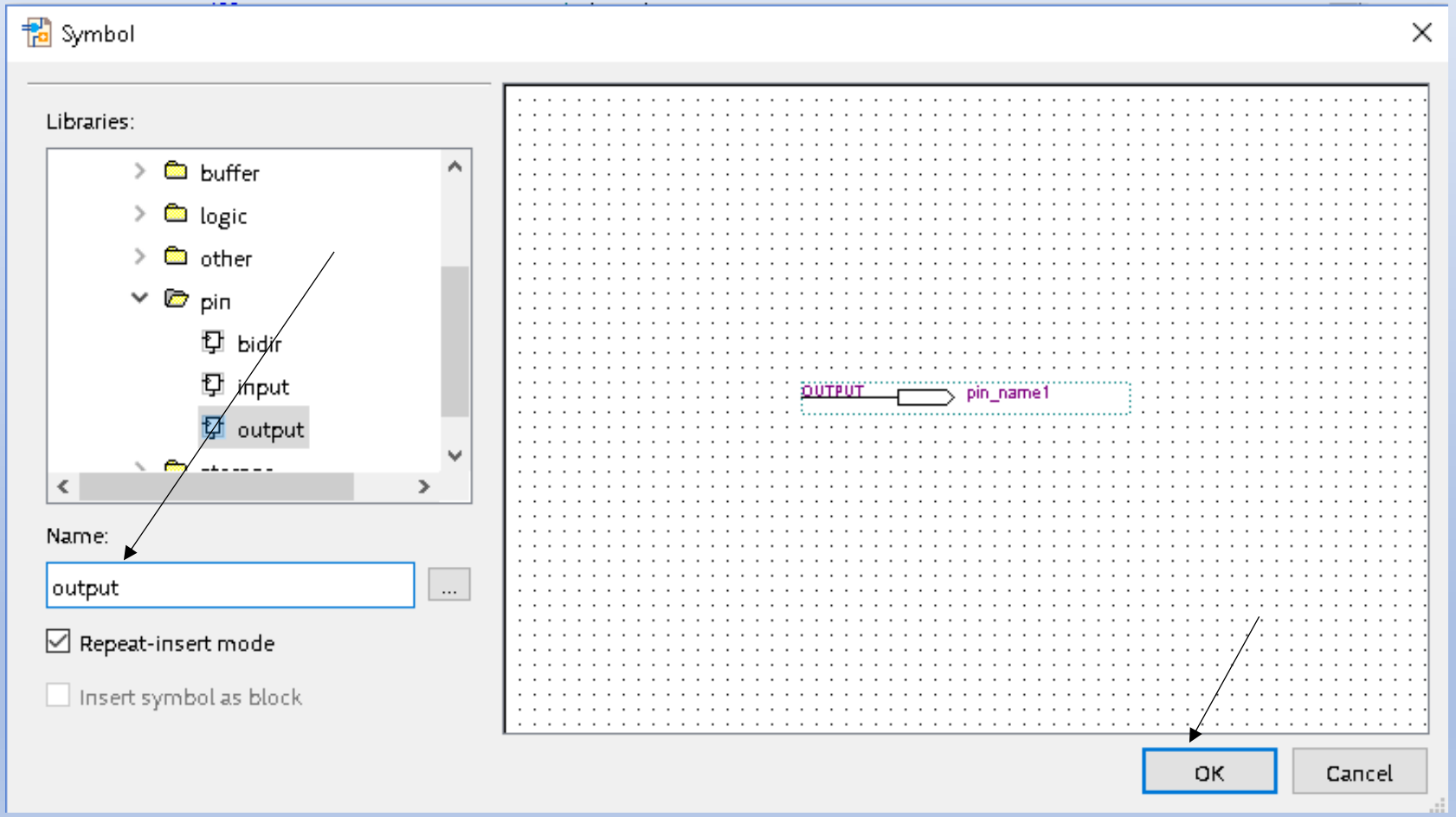
Inserir terminal de saida



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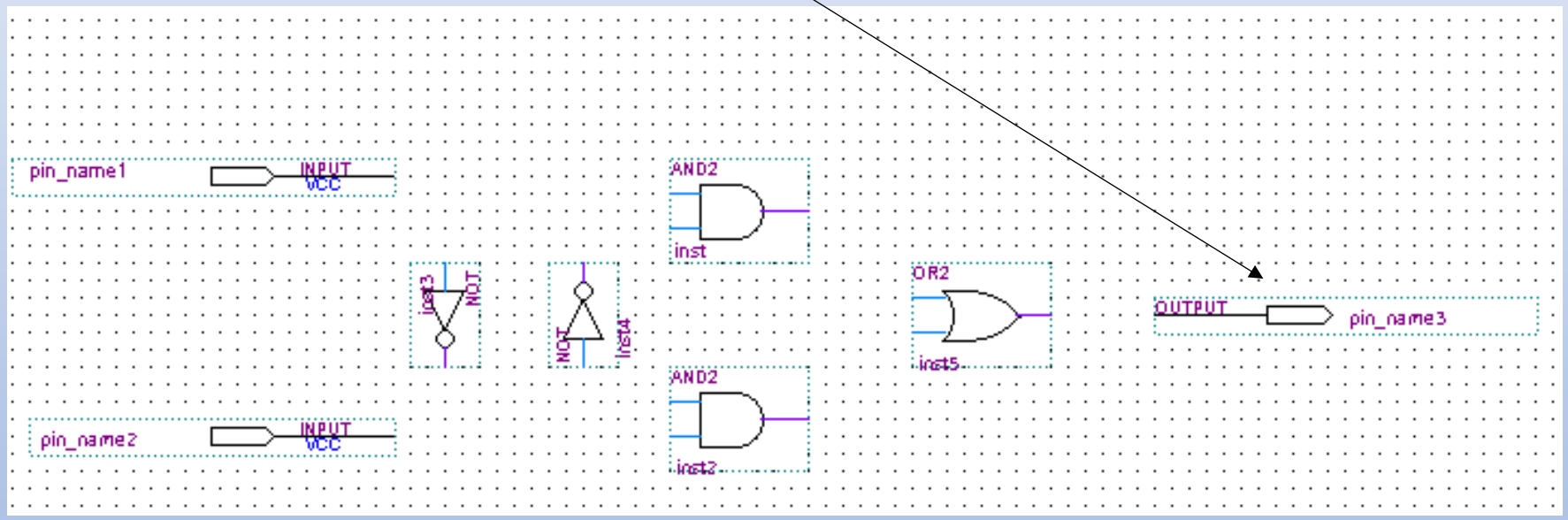
Posicione o terminal de saida



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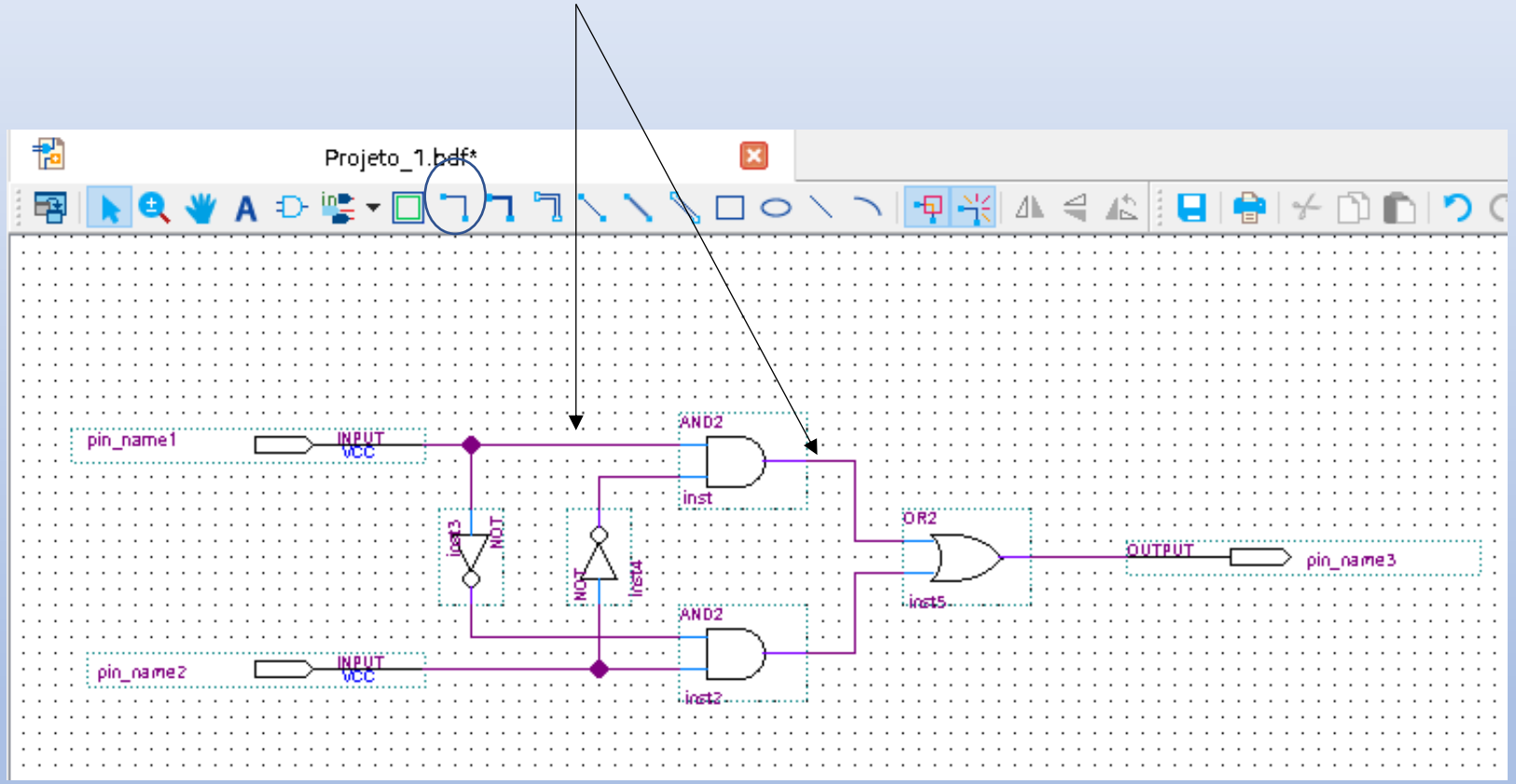
Interligação entre os componentes



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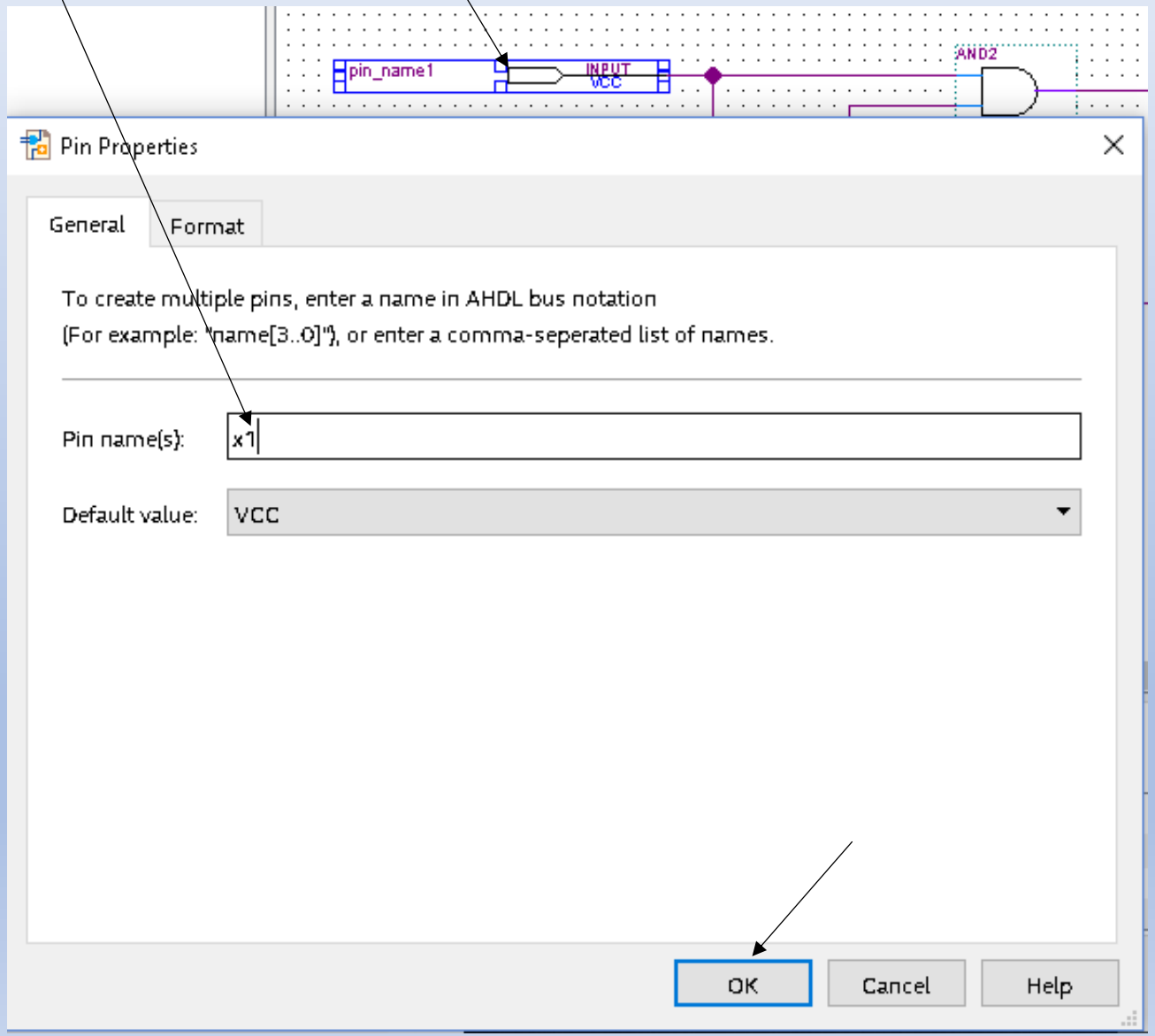
Atribuir nomes aos pinos de entrada e saida

Pin Name - duplo clique



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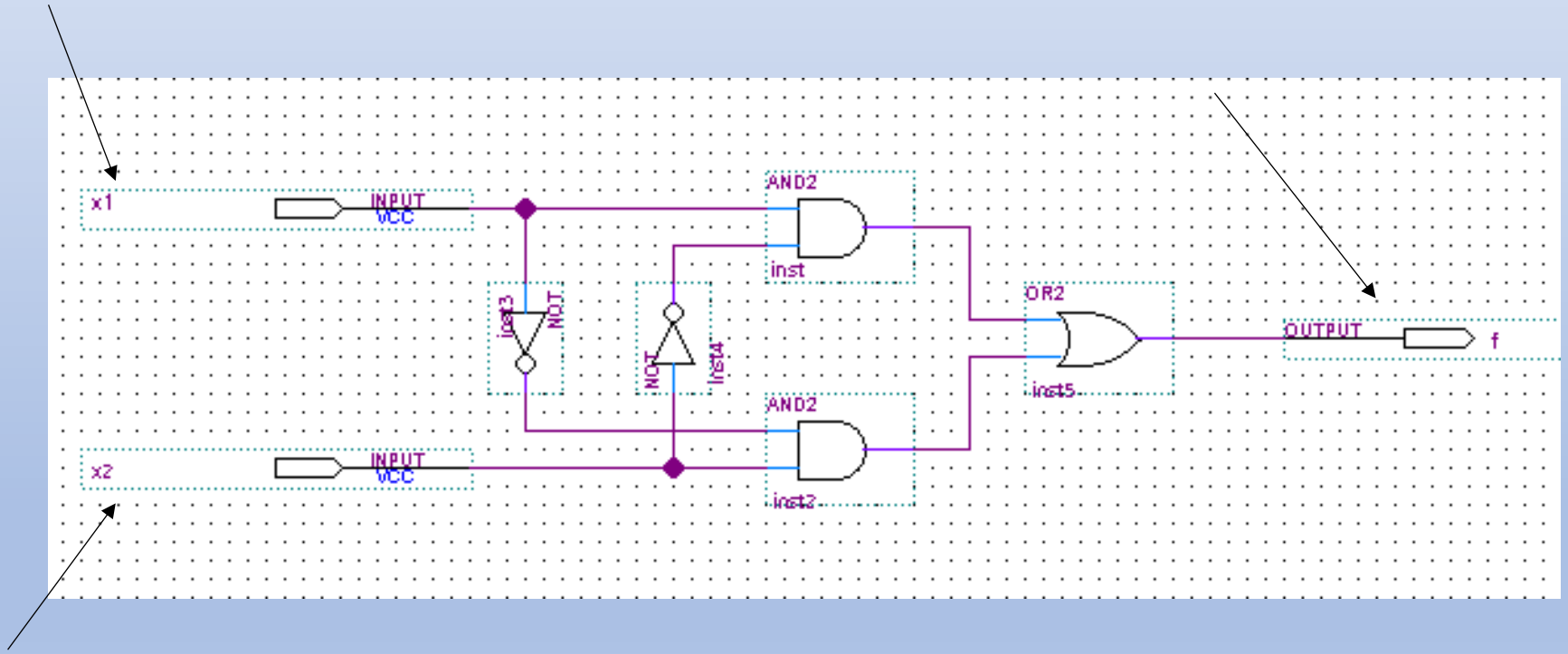
Atribuir nomes aos terminais



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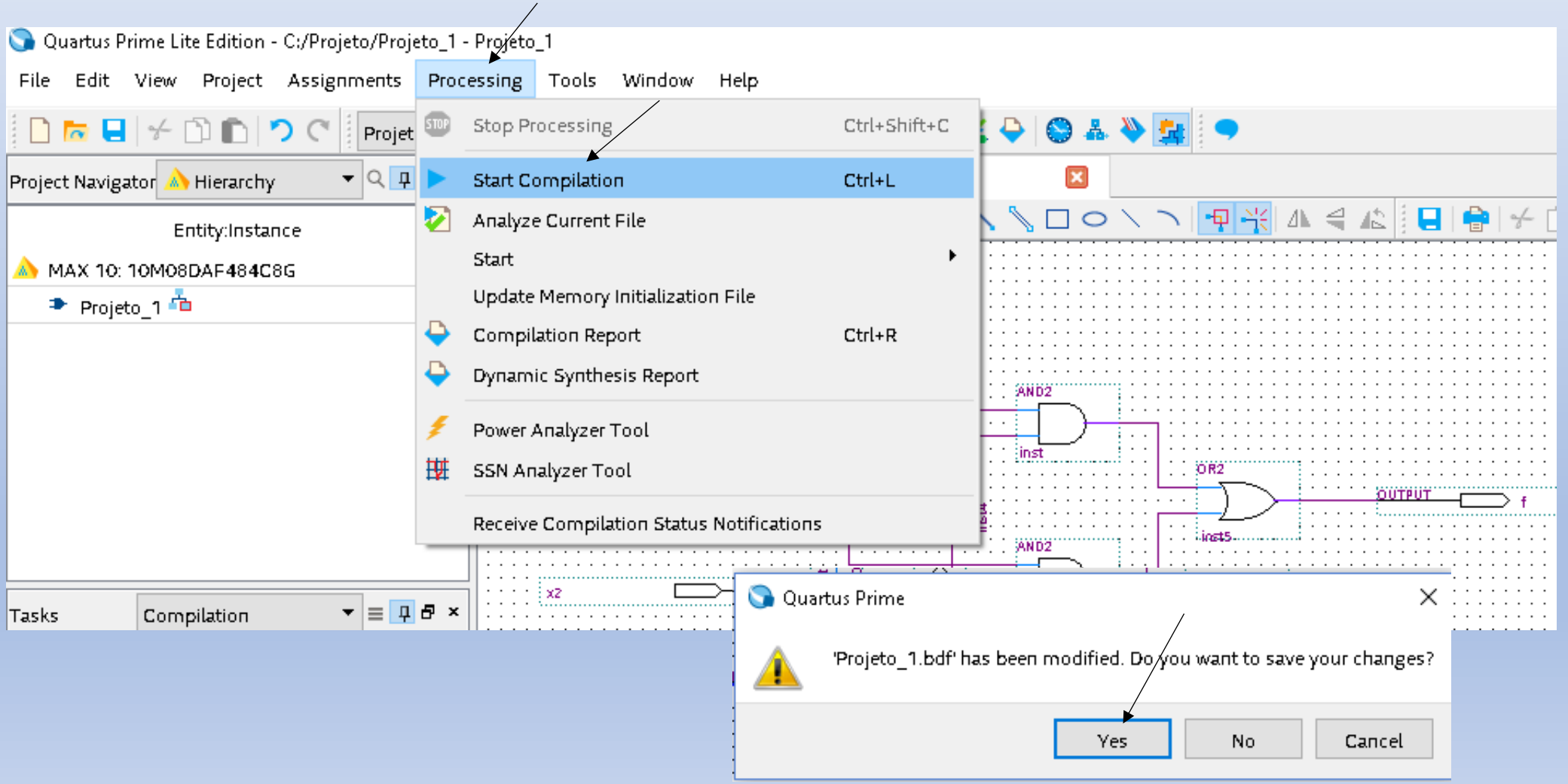
Compilação do Projeto

Processing - Start Compilation (O projeto deve ser salvo antes de compilar)



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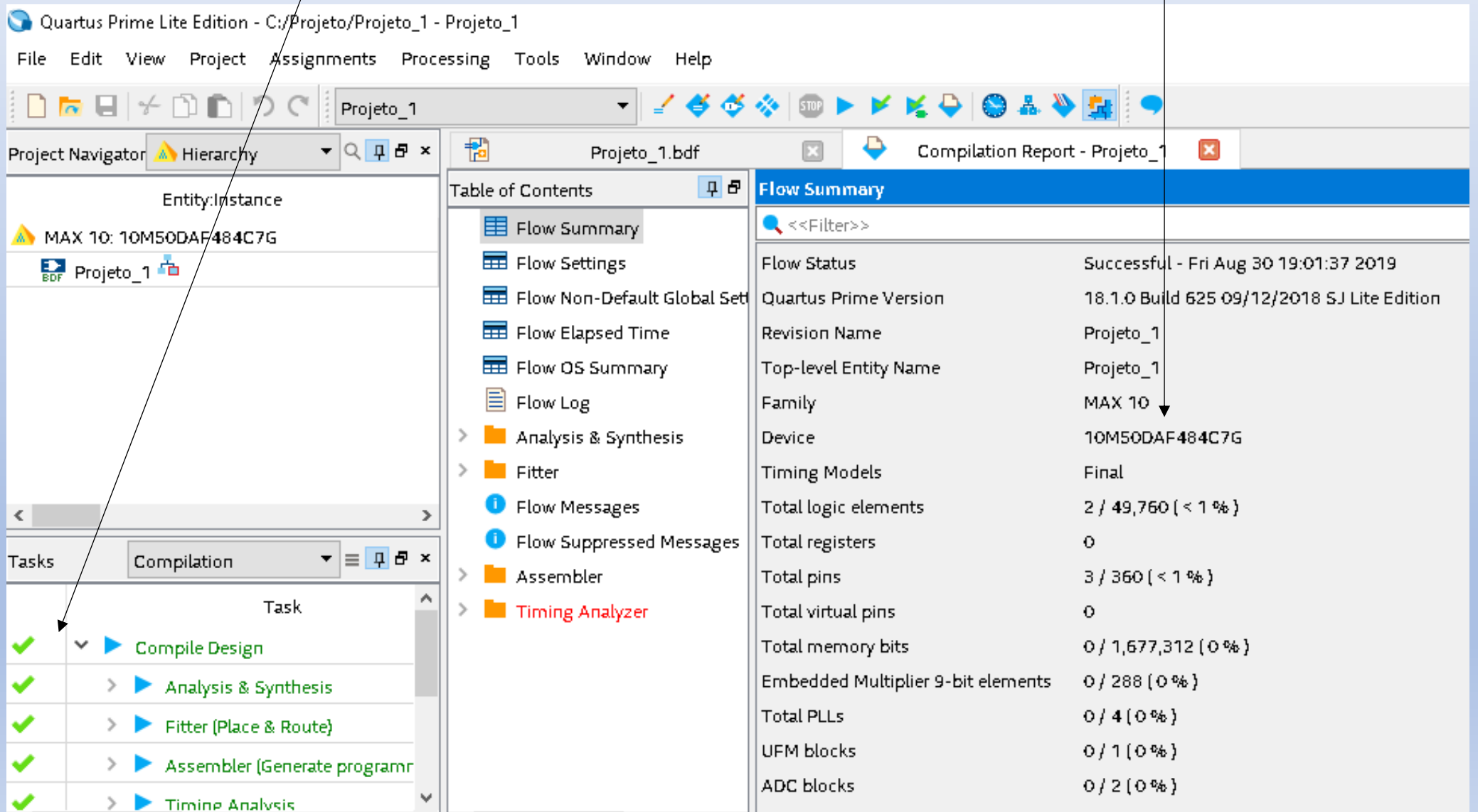
Etapas da compilação

Resumo da compilação



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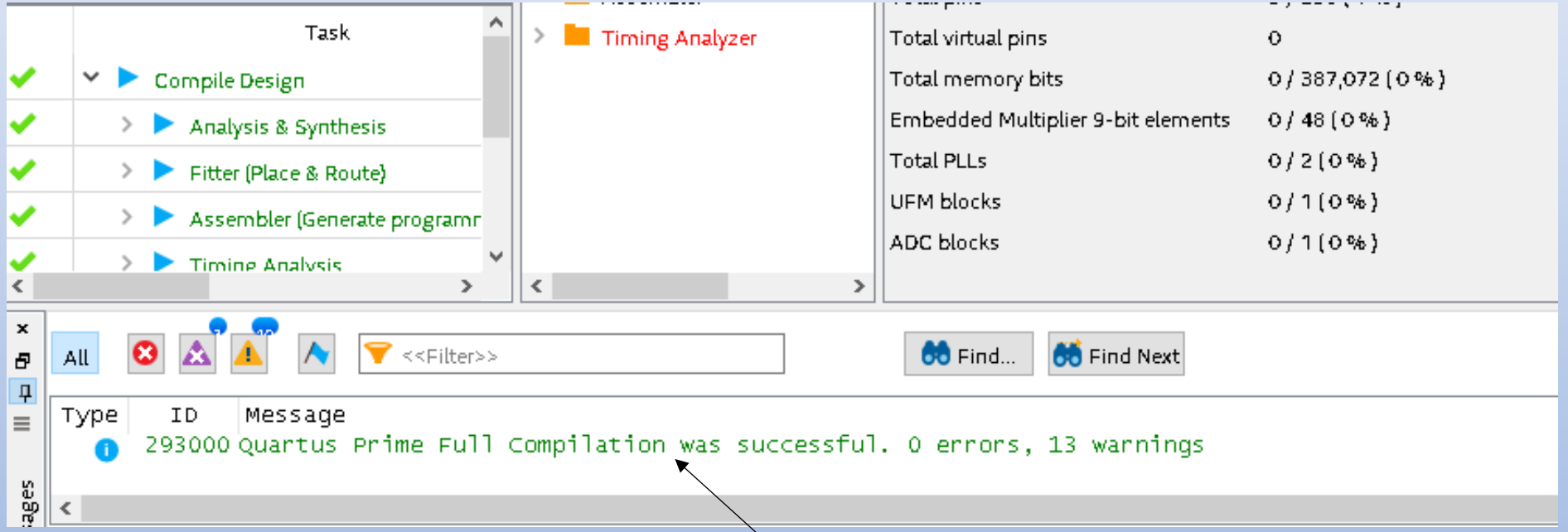
Etapas da compilação



Indicacao ou Erros quando houver.

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Vincular os Pinos do FPGA as Entradas e Saidas do Pojeto

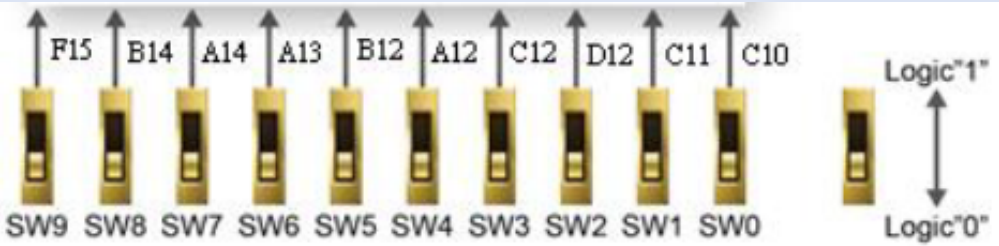

Figure 3-15 Connections between the slide switches and MAX 10 FPGA

Table 3-4 Pin Assignment of Slide Switches

Signal Name	FPGA Pin No.	Description	I/O Standard
SW0	PIN_C10	Slide Switch[0]	3.3-V LVTTL
SW1	PIN_C11	Slide Switch[1]	3.3-V LVTTL
SW2	PIN_D12	Slide Switch[2]	3.3-V LVTTL
SW3	PIN_C12	Slide Switch[3]	3.3-V LVTTL
SW4	PIN_A12	Slide Switch[4]	3.3-V LVTTL
SW5	PIN_B12	Slide Switch[5]	3.3-V LVTTL
SW6	PIN_A13	Slide Switch[6]	3.3-V LVTTL
SW7	PIN_A14	Slide Switch[7]	3.3-V LVTTL
SW8	PIN_B14	Slide Switch[8]	3.3-V LVTTL
SW9	PIN_F15	Slide Switch[9]	3.3-V LVTTL

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Vincular os Pinos do FPGA as Entradas e Saidas do Pojeto

Table 3-5 Pin Assignment of LEDs

Signal Name	FPGA Pin No.	Description	I/O Standard
LEDR0	PIN_A8	LED [0]	3.3-V LVTTL
LEDR1	PIN_A9	LED [1]	3.3-V LVTTL
LEDR2	PIN_A10	LED [2]	3.3-V LVTTL
LEDR3	PIN_B10	LED [3]	3.3-V LVTTL
LEDR4	PIN_D13	LED [4]	3.3-V LVTTL
LEDR5	PIN_C13	LED [5]	3.3-V LVTTL
LEDR6	PIN_E14	LED [6]	3.3-V LVTTL
LEDR7	PIN_D14	LED [7]	3.3-V LVTTL
LEDR8	PIN_A11	LED [8]	3.3-V LVTTL
LEDR9	PIN_B11	LED [9]	3.3-V LVTTL

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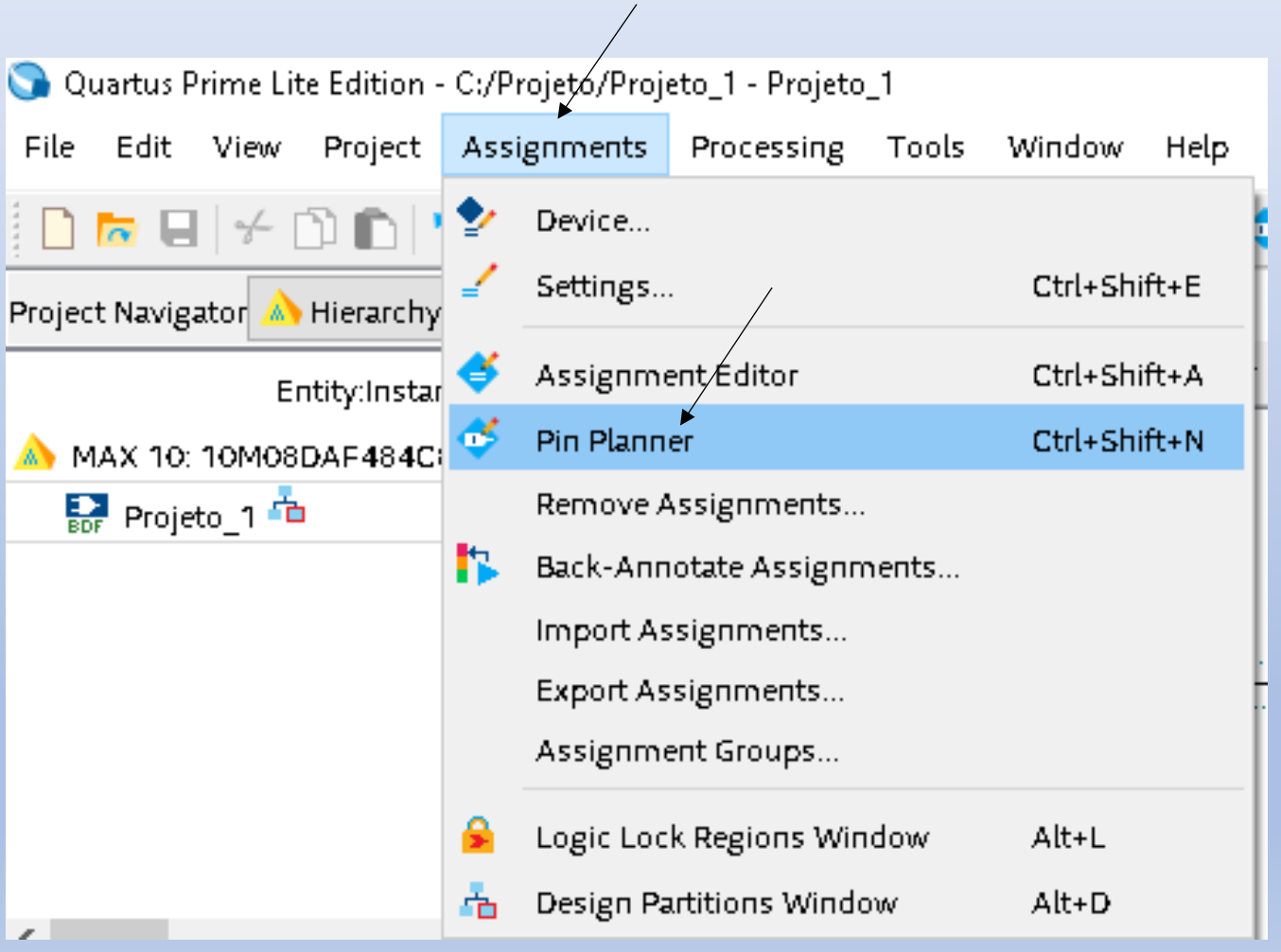
Vincular os Pinos do FPGA as Entradas e Saidas do Pojeto

Assignments – Pin Planner



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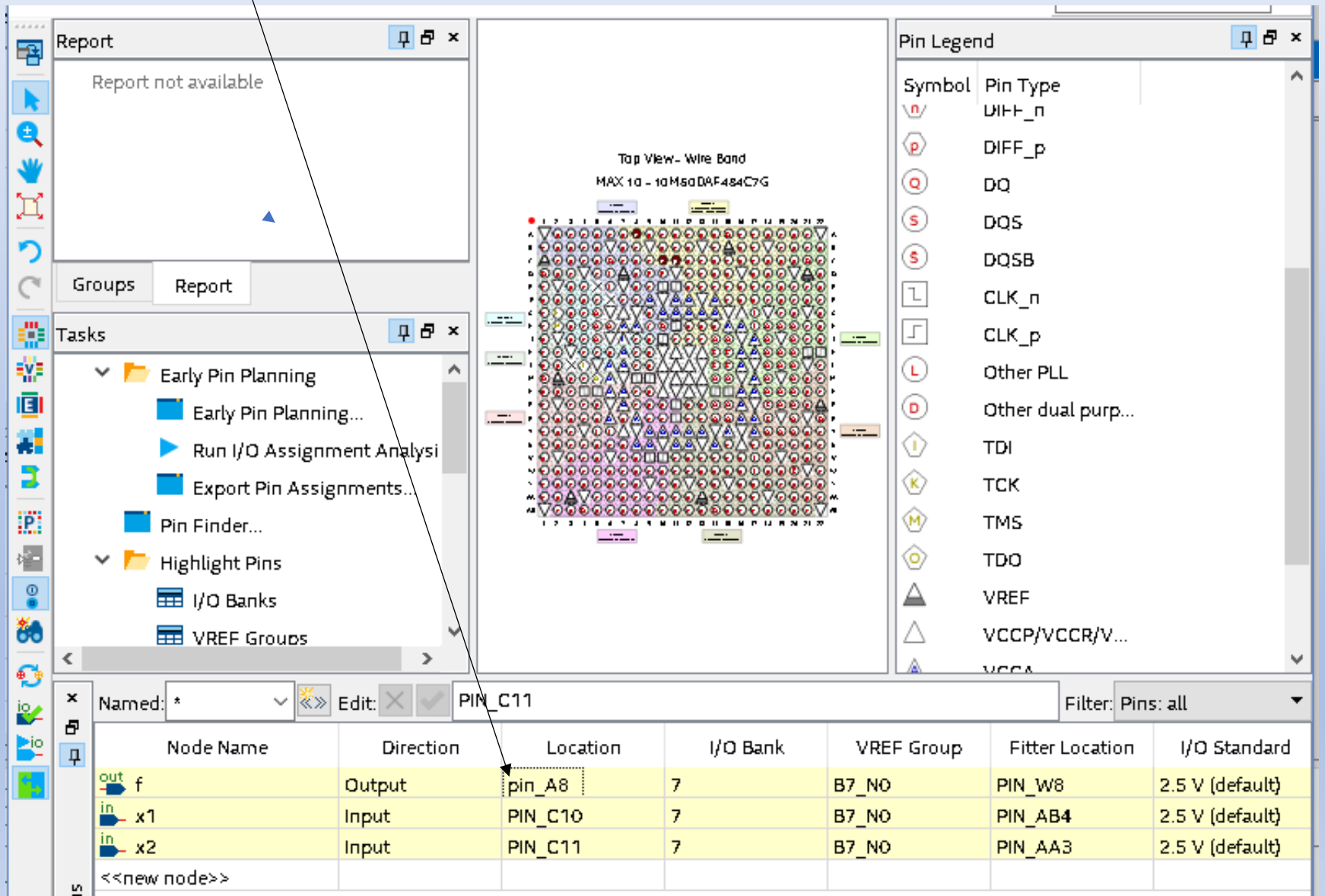
F – PIN_A8, x1 – PIN_C10 e PIN_C11



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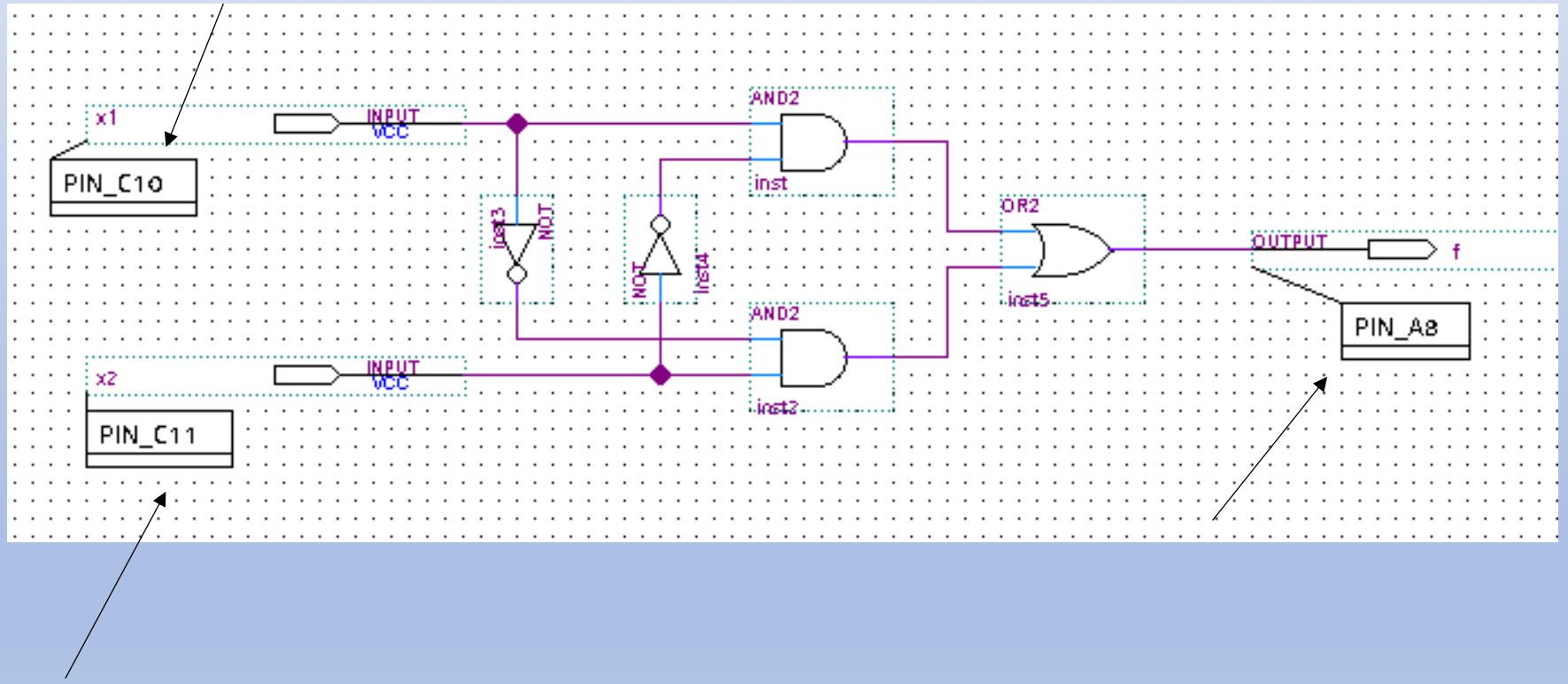
Compilar o Projeto novamente

Processing – Start Compilation



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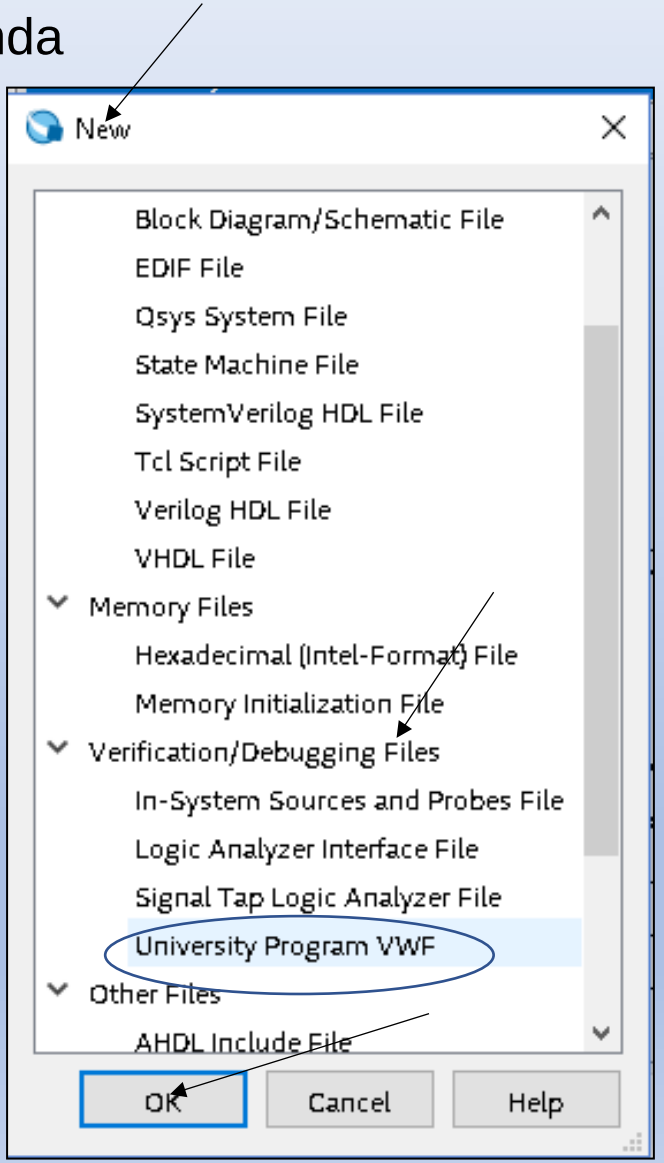
Simulacao Funcional do Circuito

Criacao dos Vetores de Testes – Formas de Onda

File – New – Verification/Debugging Files – University Program VWF



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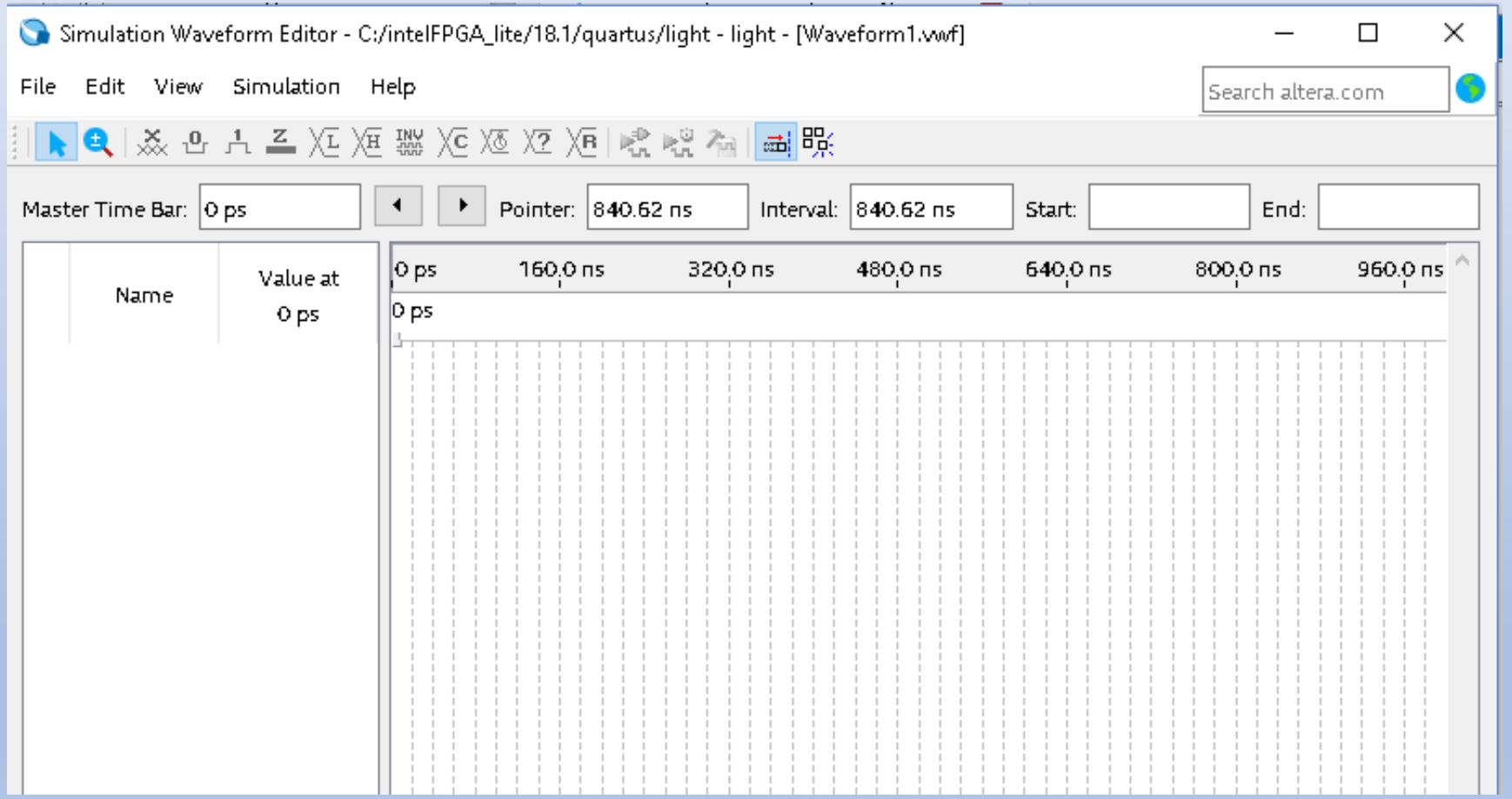
Tela do Editor de Forma de Ondas



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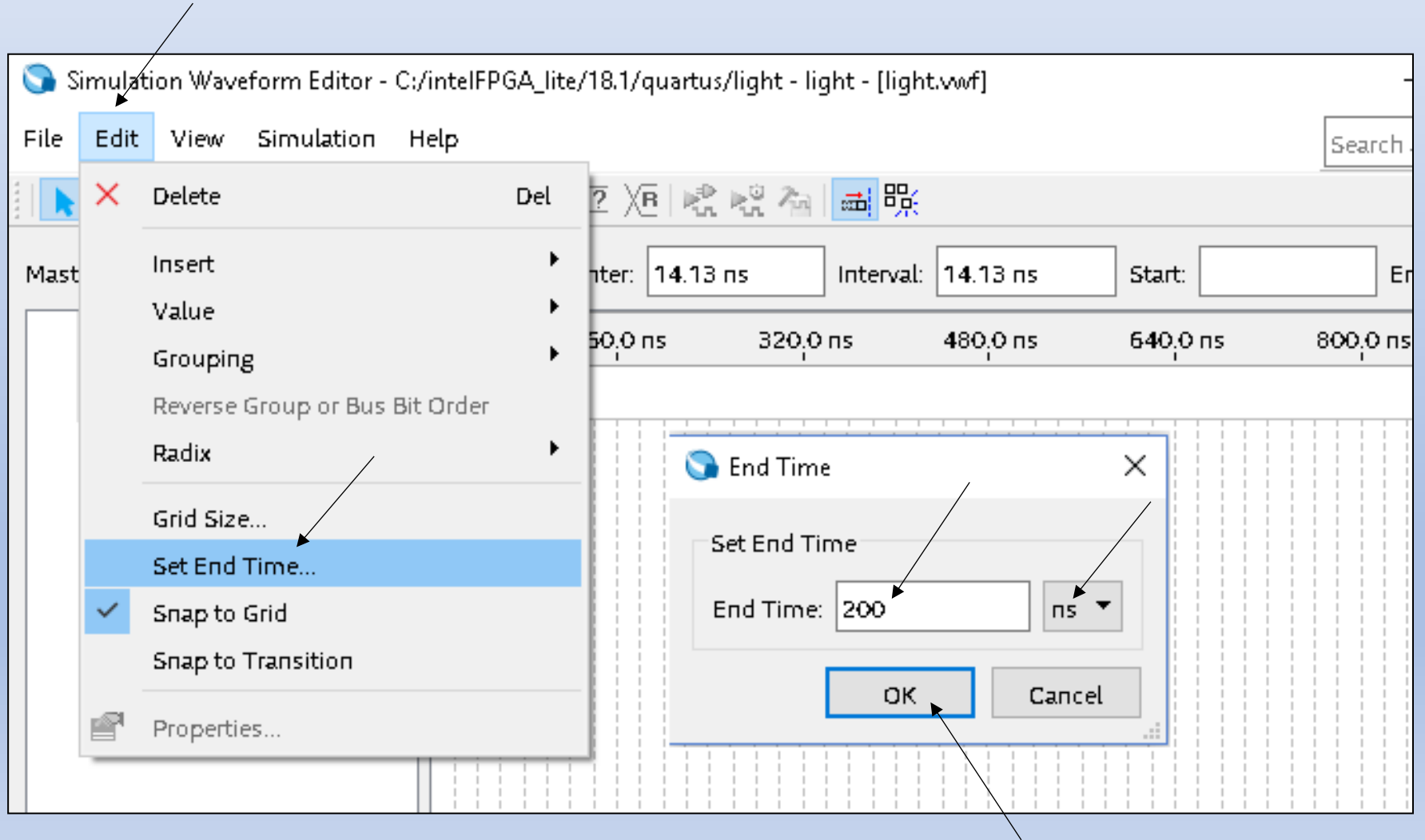
Configure o tempo de Simulacao de 0 a 200 ns

Edit – Set End Time



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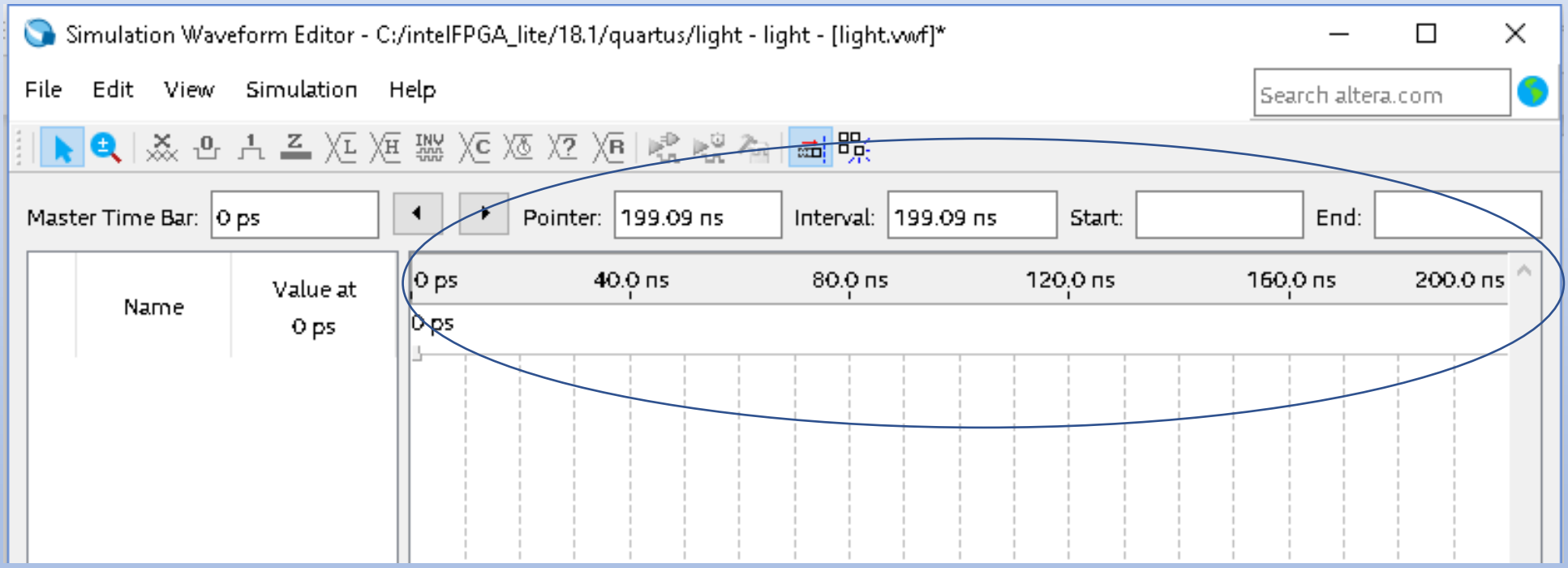
Editor de Forma de Ondas



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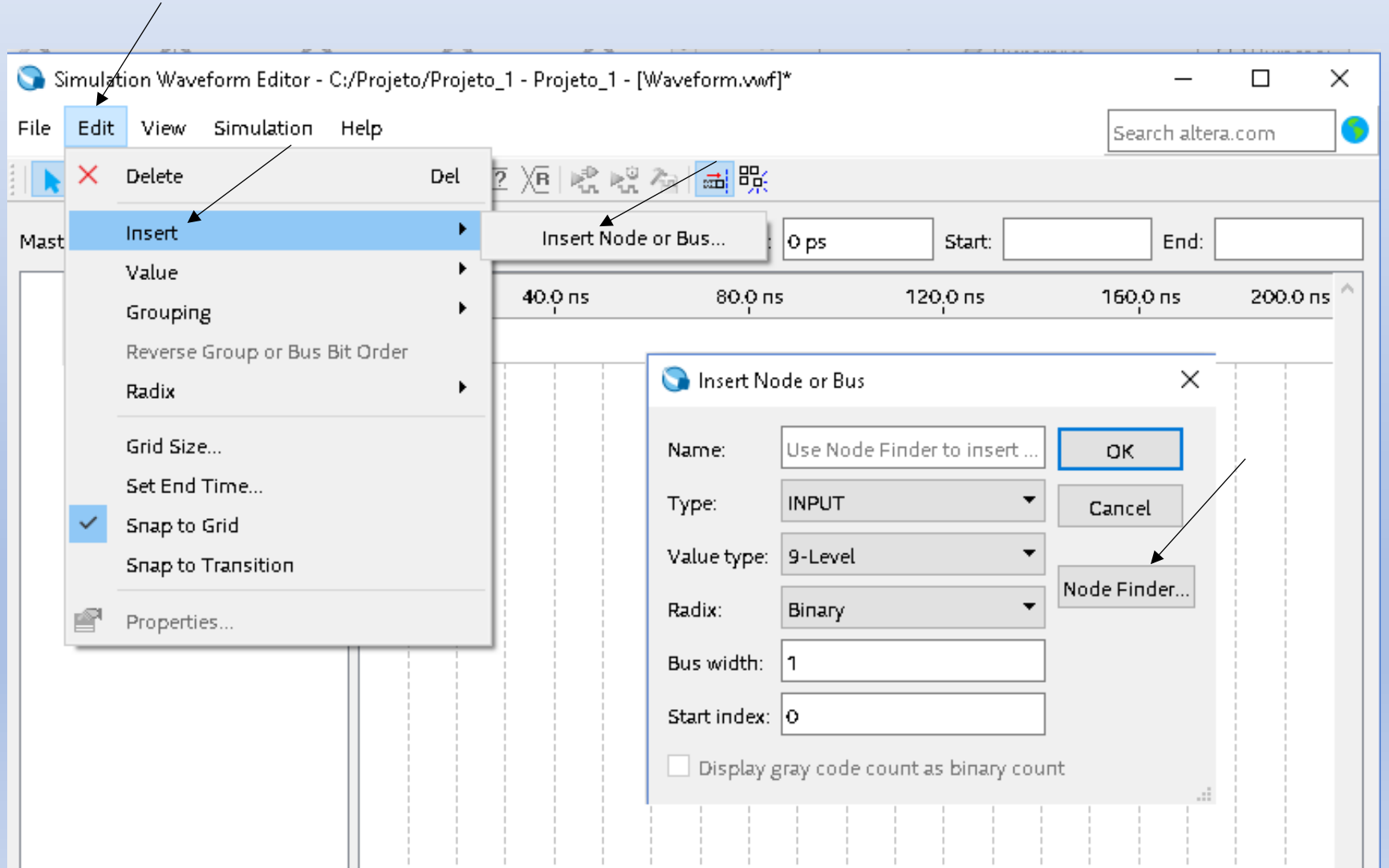
Incluir as entradas e saidas no Editor de Forma de Ondas

Edit – Insert – Inset Node or Bus – Node Finder



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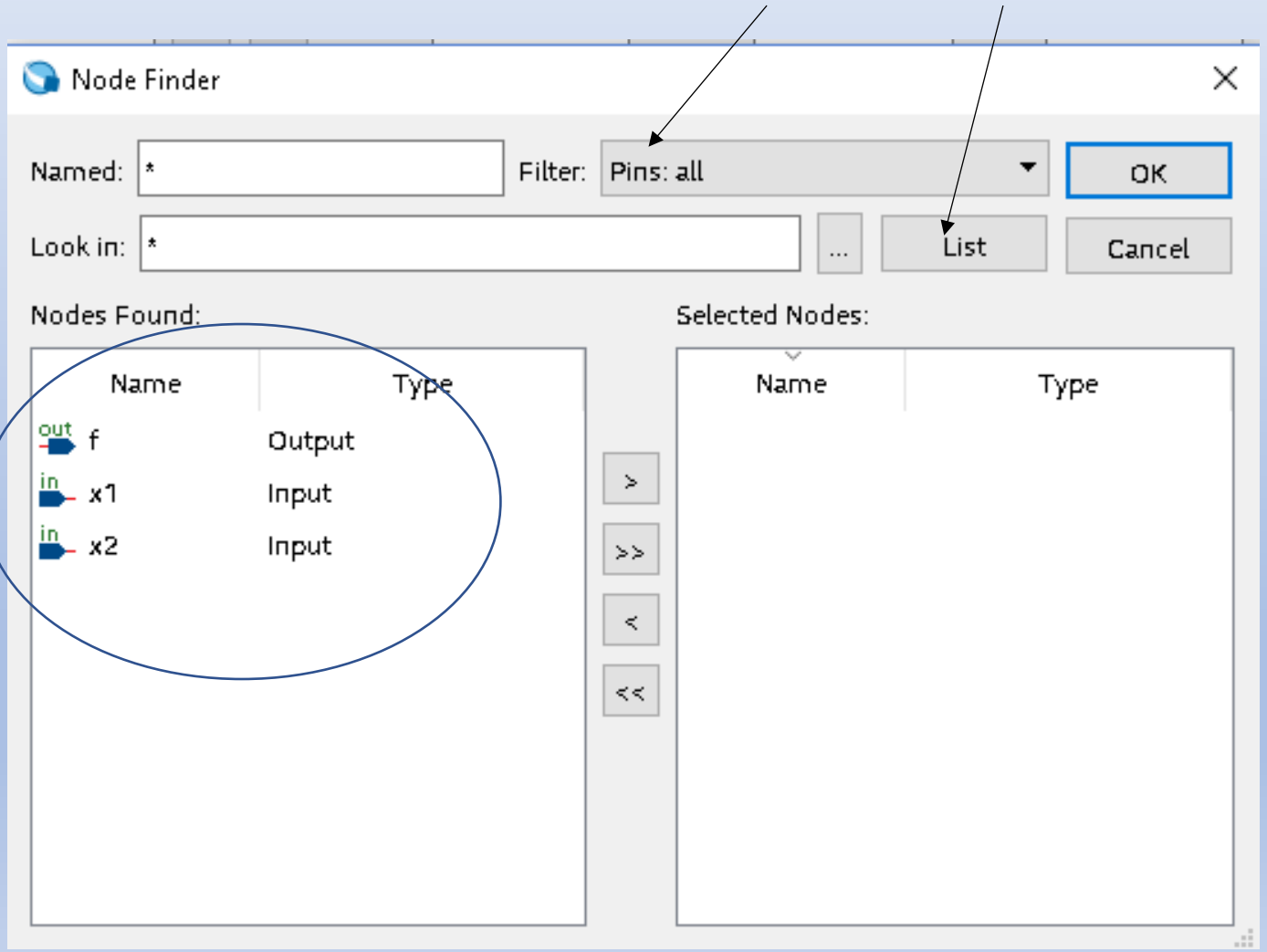
Indicacao das Entradas e Saidas

Pins: all - List



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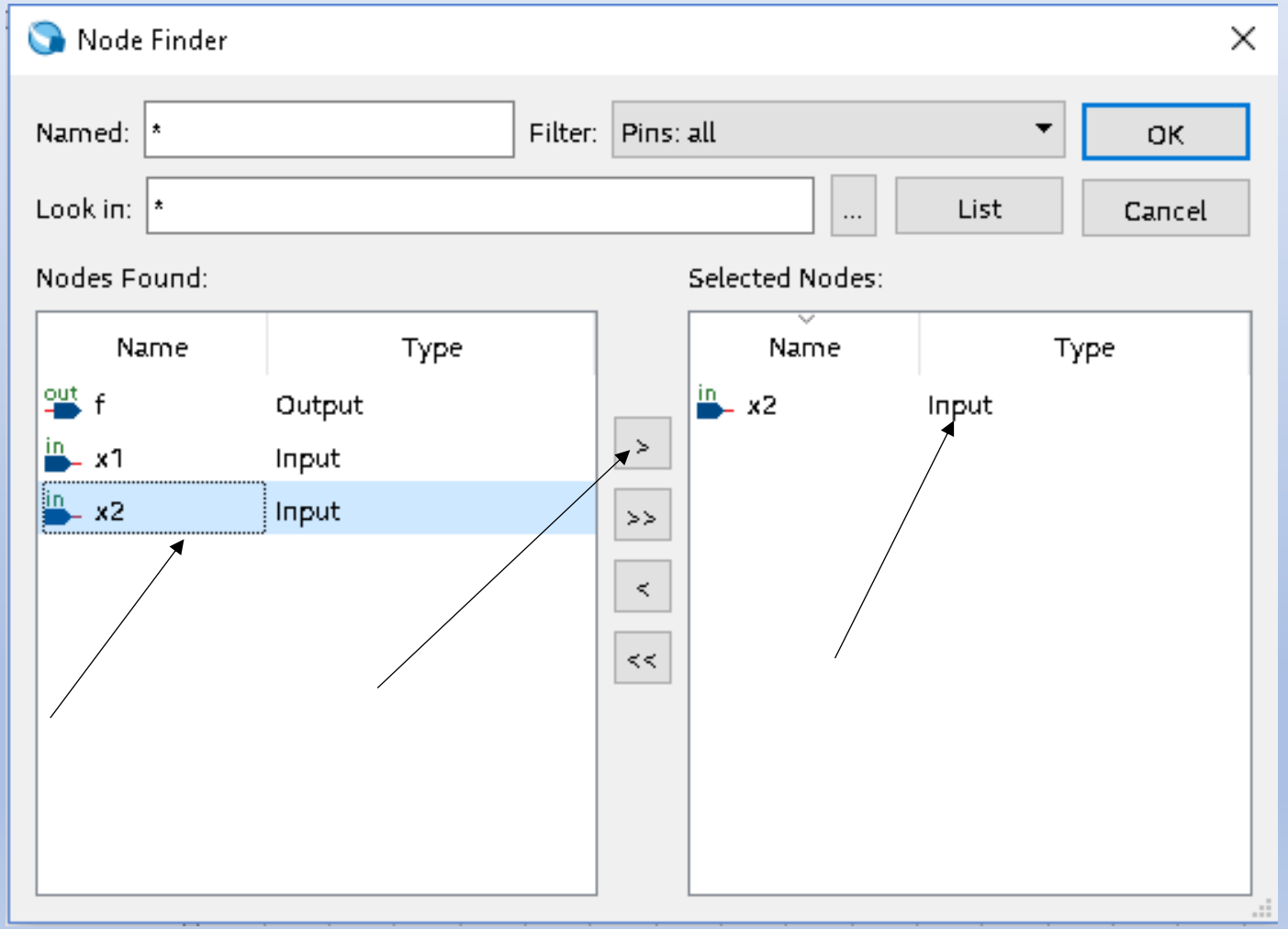
Selecionando a entrada x2 para Simulacao



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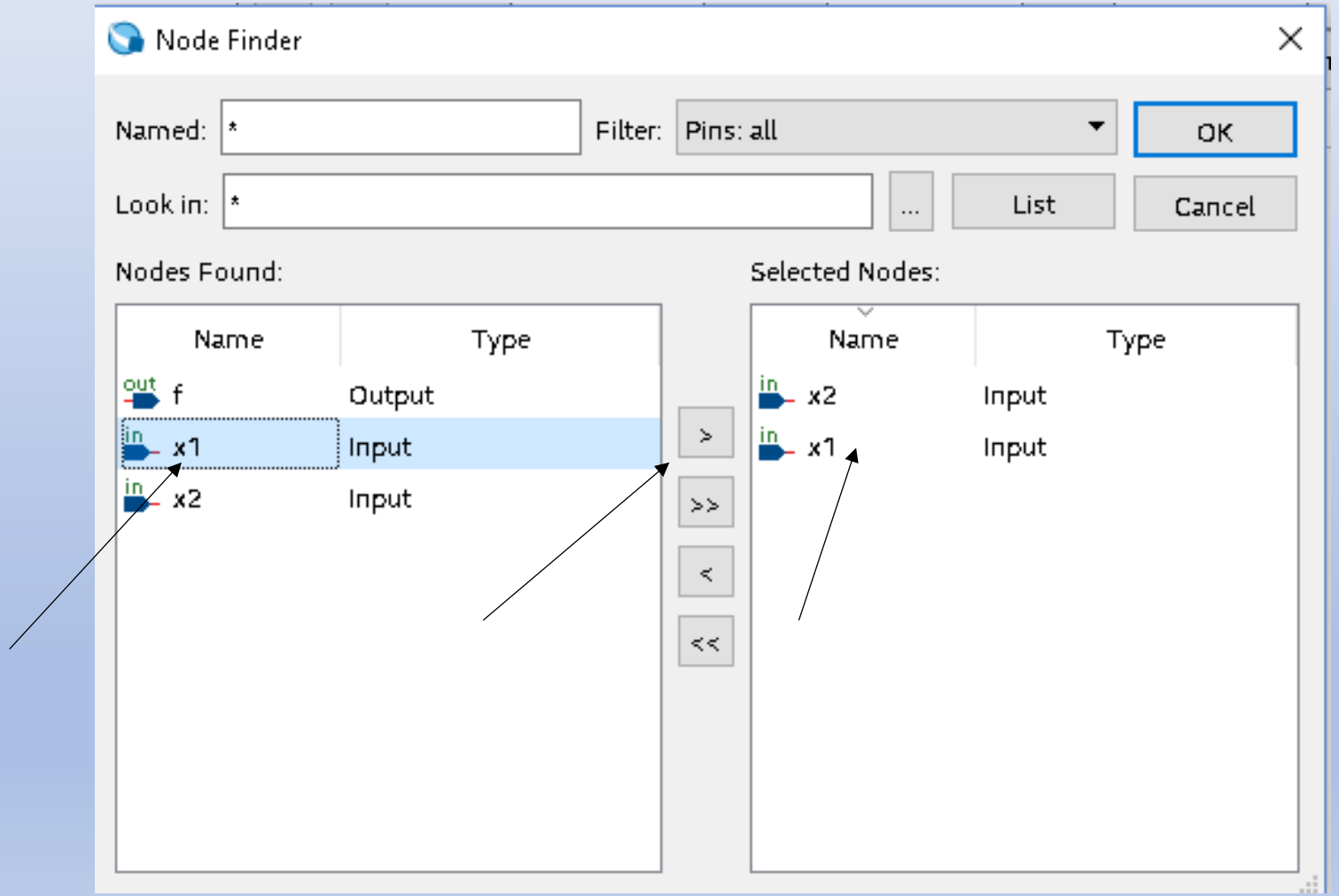
Selecionando a entrada x1 para Simulacao



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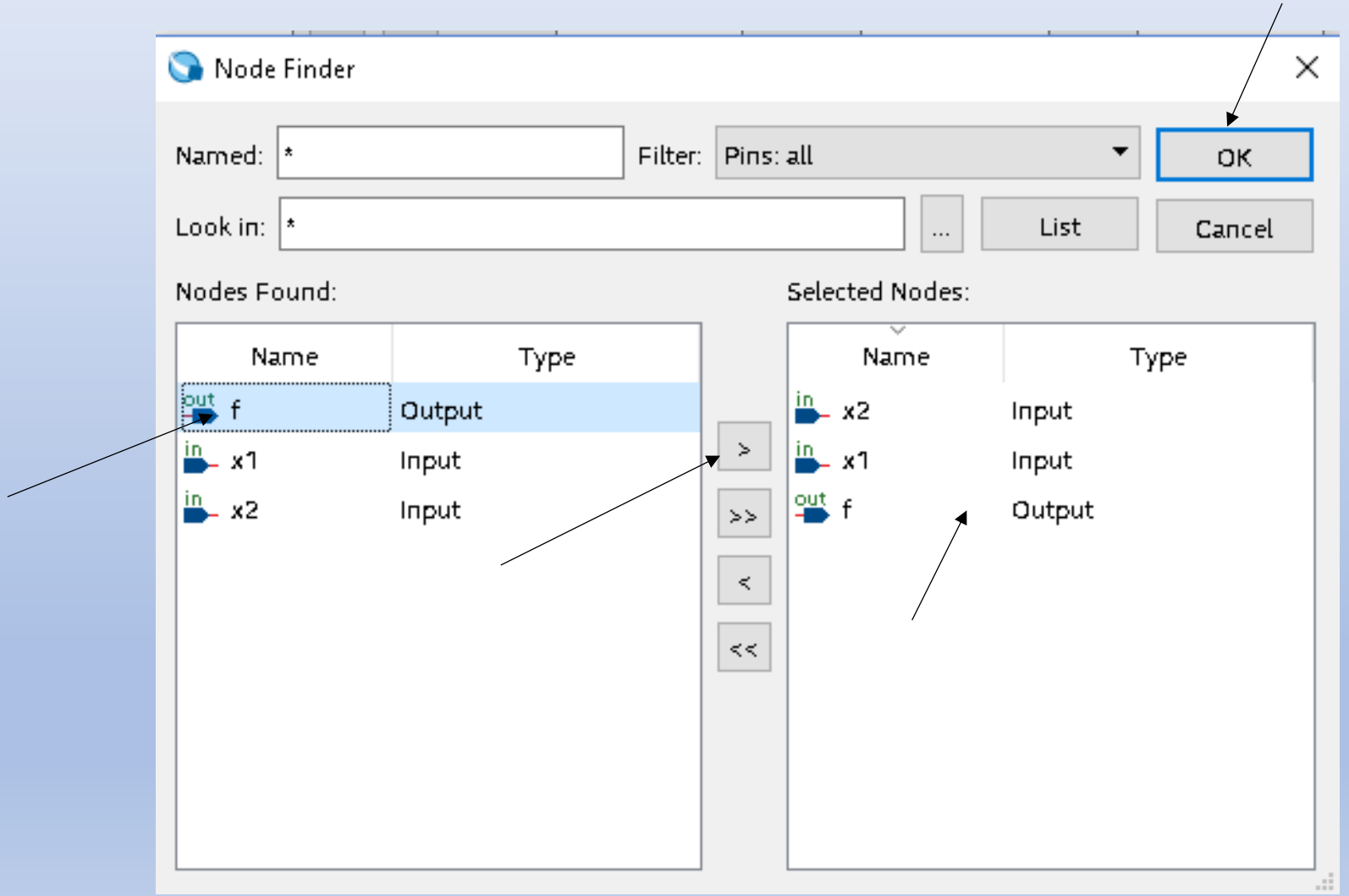
Selecionando a saida f para Simulacao



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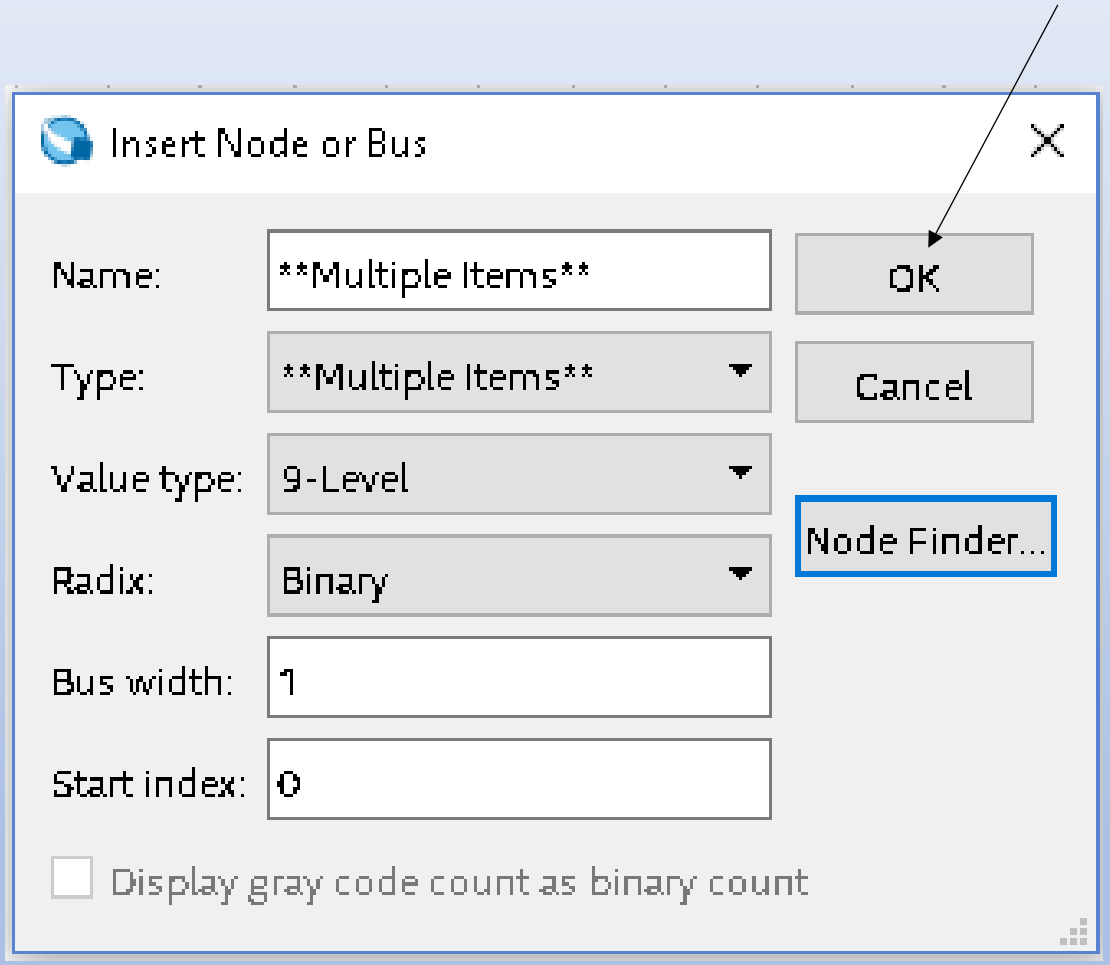

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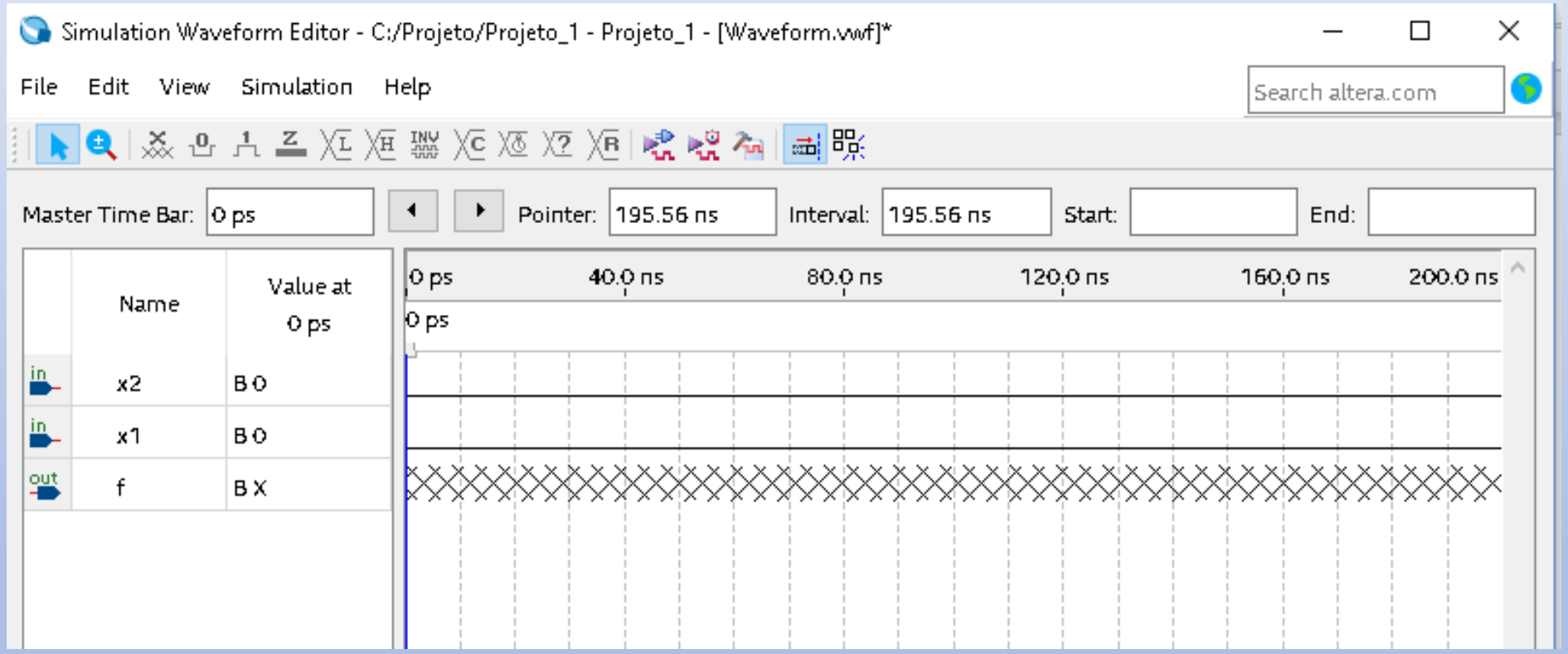
Entradas e Saidas no Editor de Formas de Ondas



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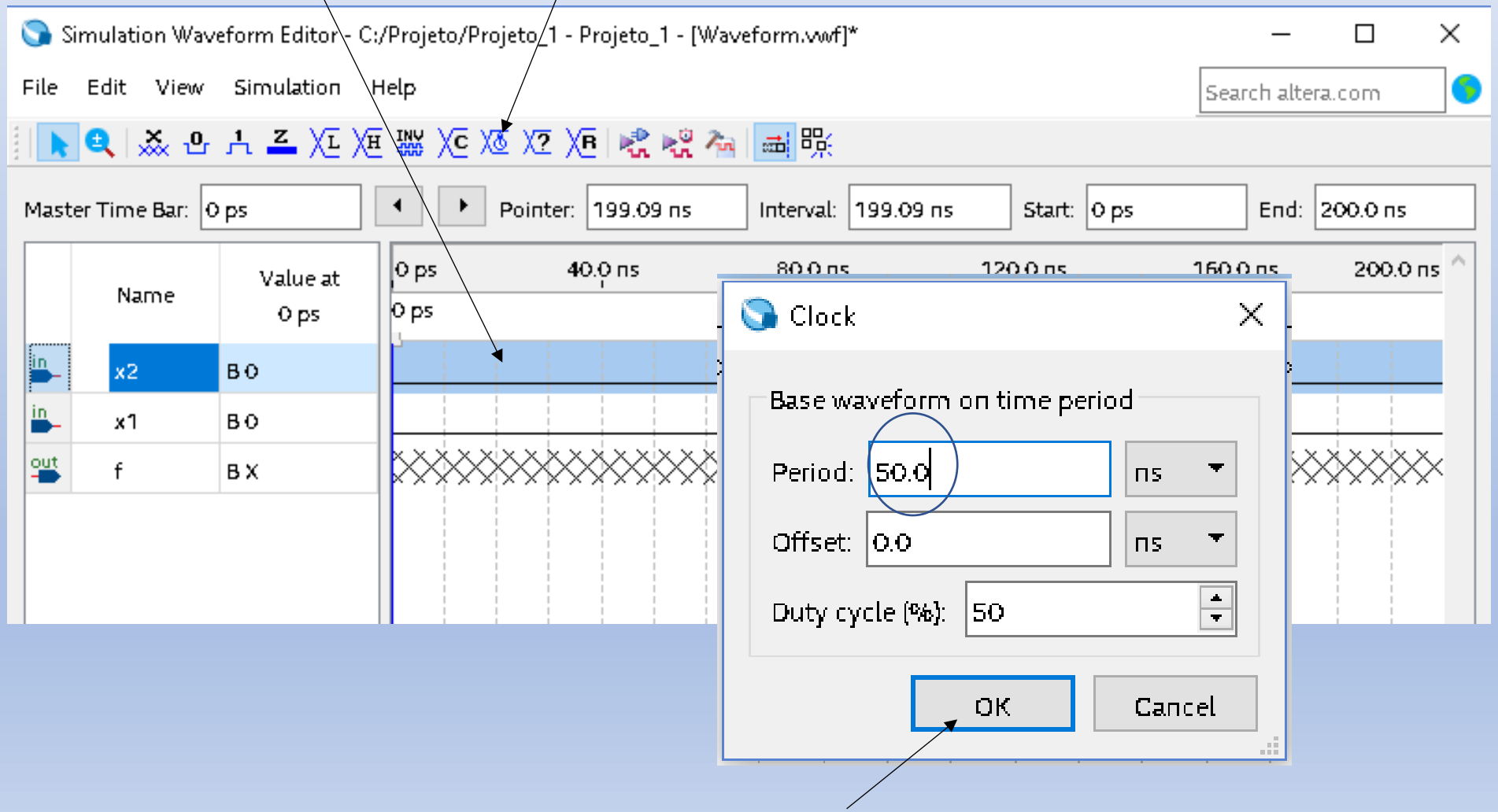
Selecione a Entrada x2 - Sinal de OverwriterClock



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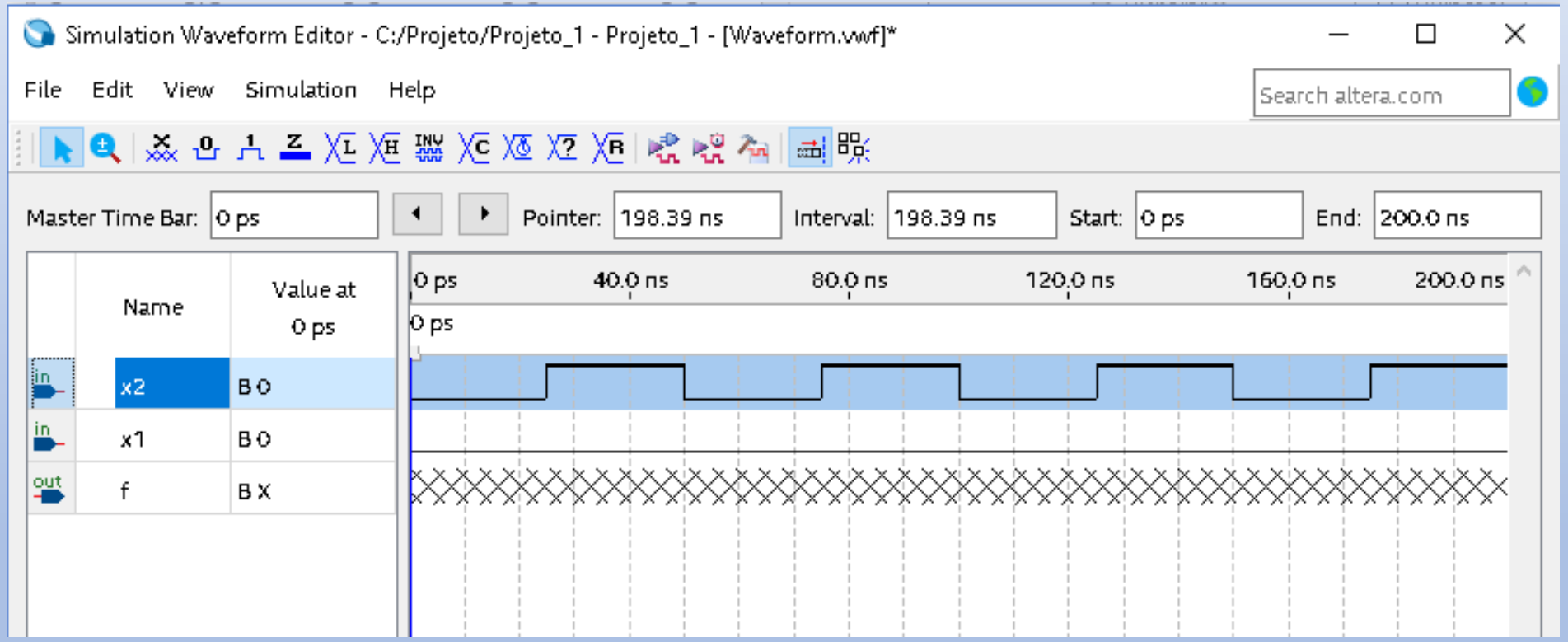
Selecione a Entrada x2 - Sinal de Clock C



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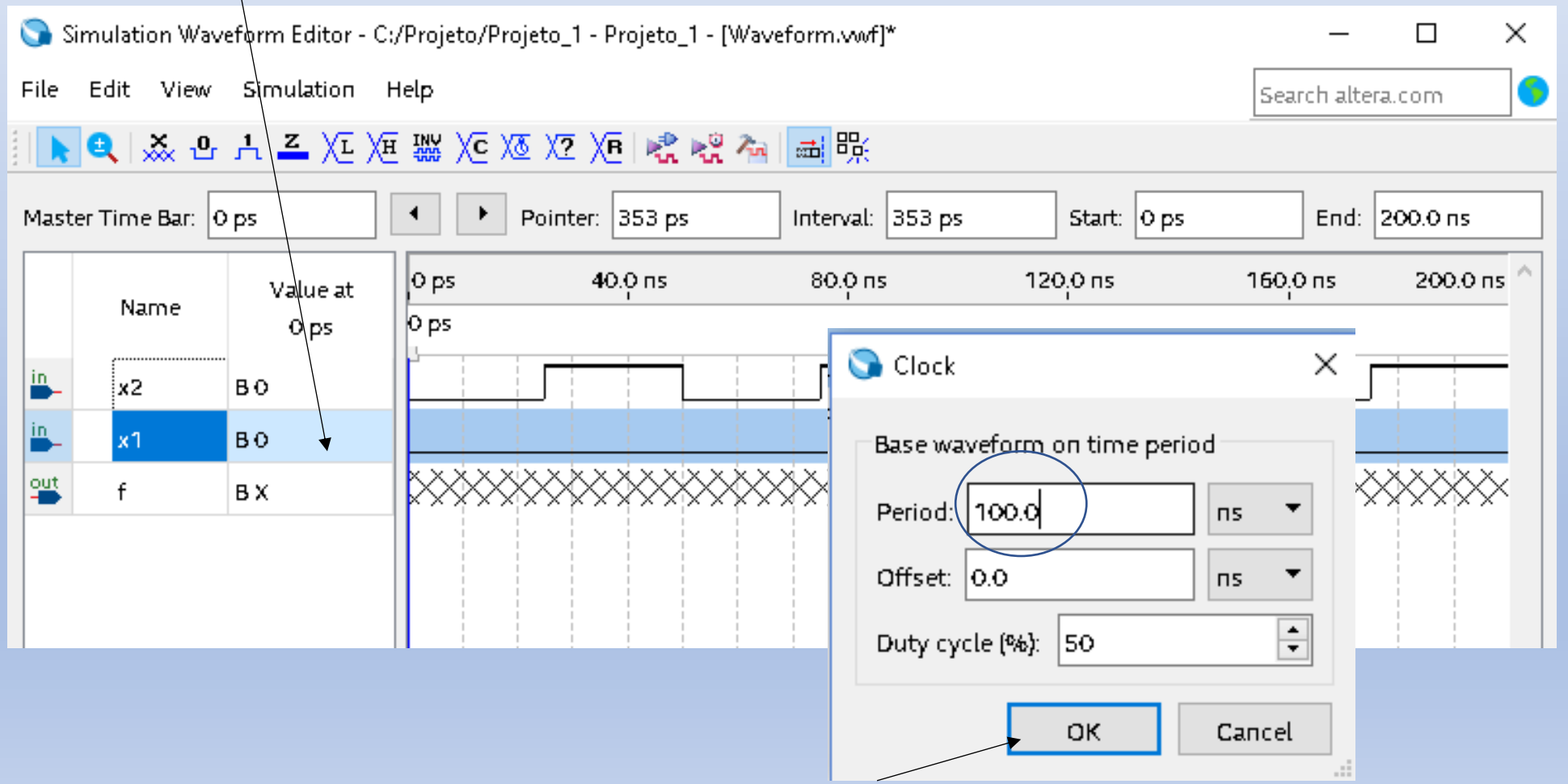
Selecione a Entrada x1 - Sinal de OverwriterClock



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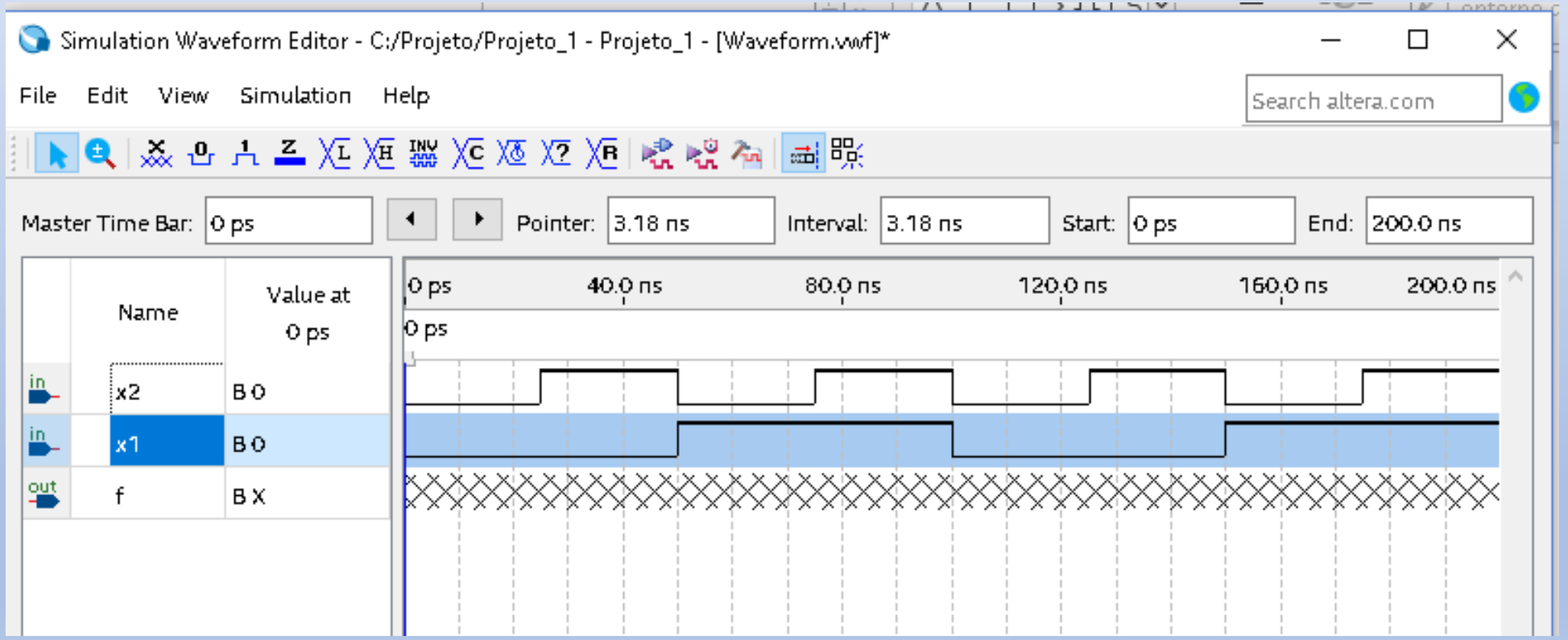
Selecione a Entrada x1 - Sinal de OverwriterClock

Salvar o Projeto_1 no diretorio C:/Projeto



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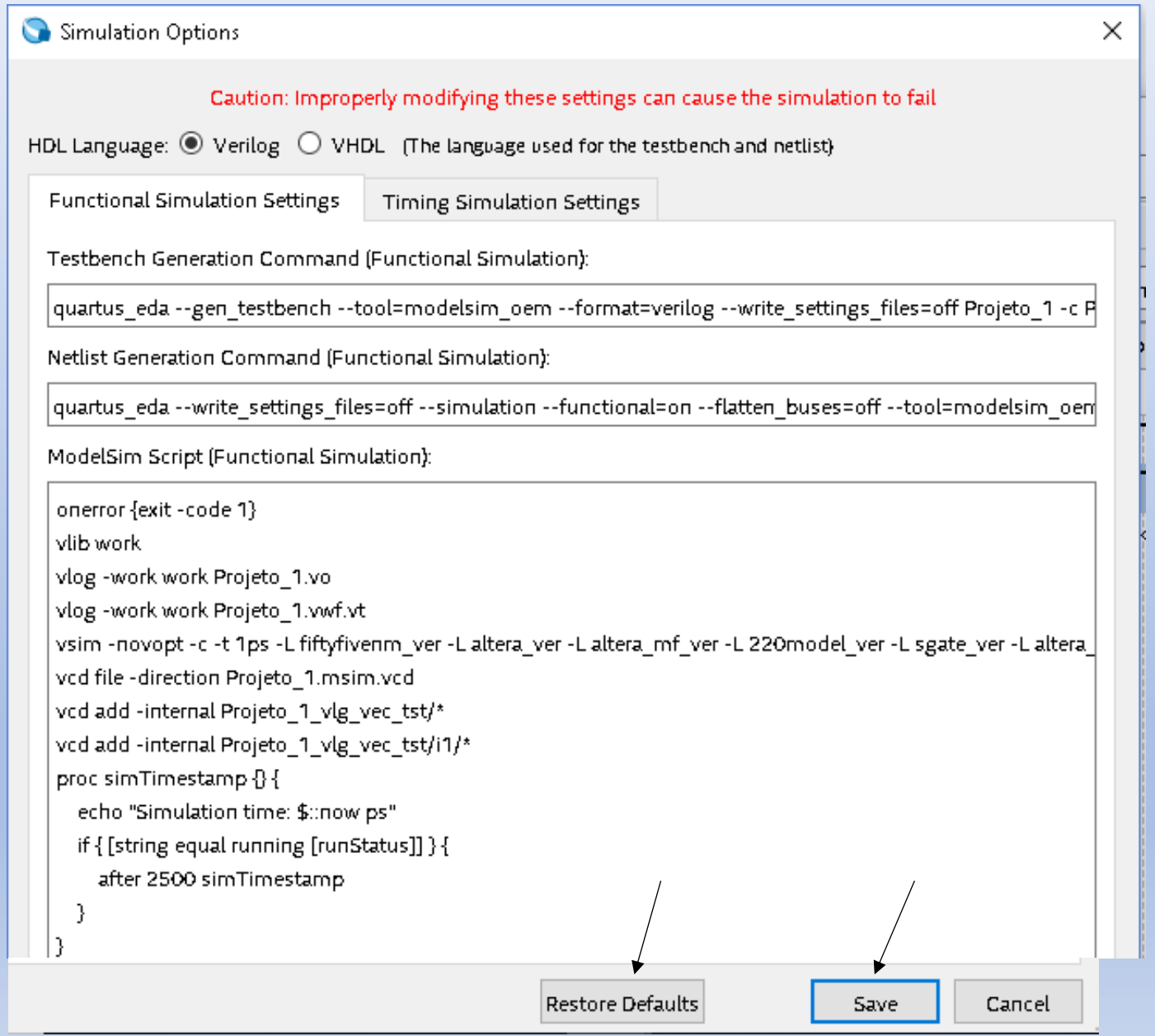

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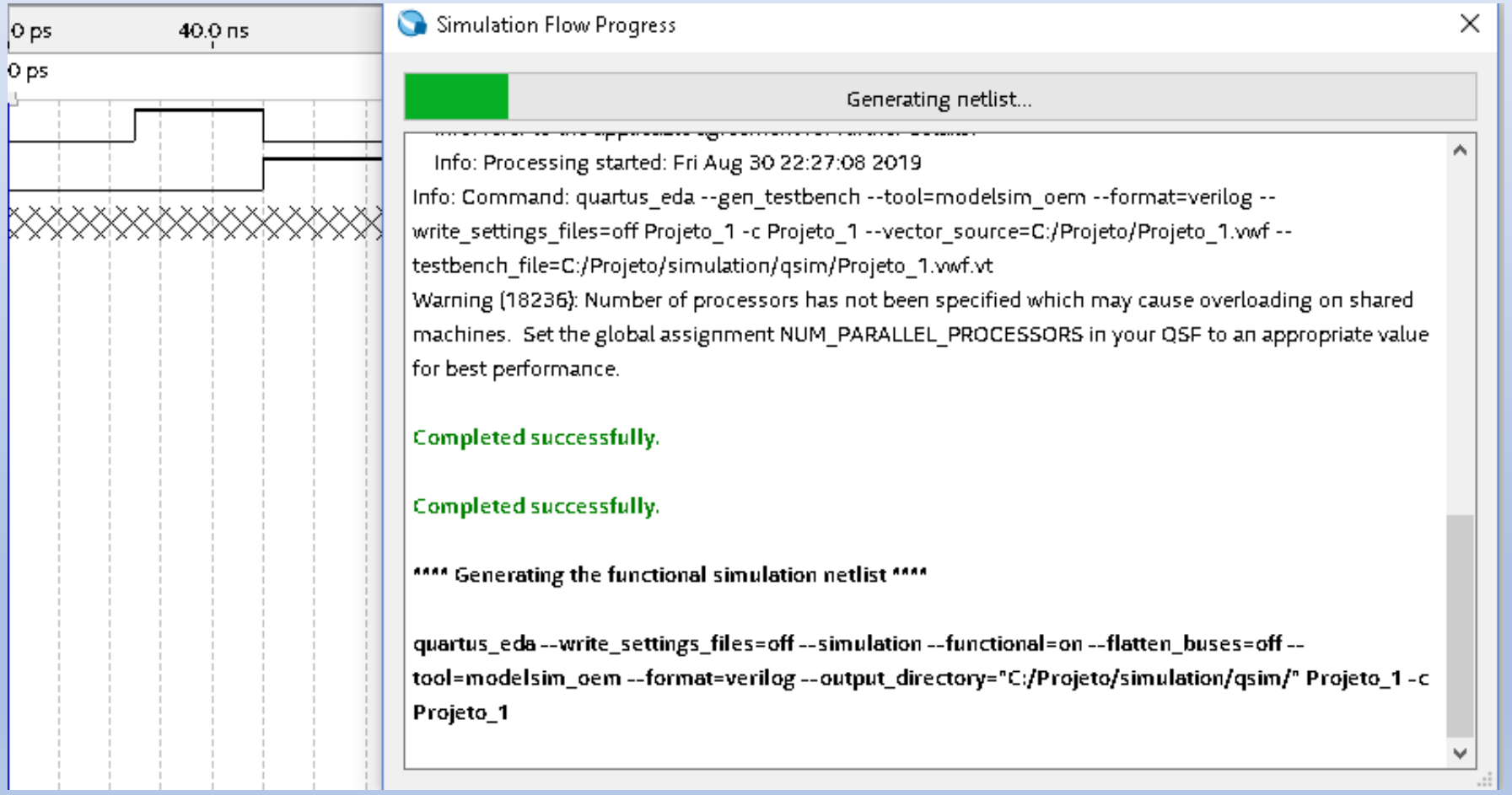
Tool - Run Functional Simulation



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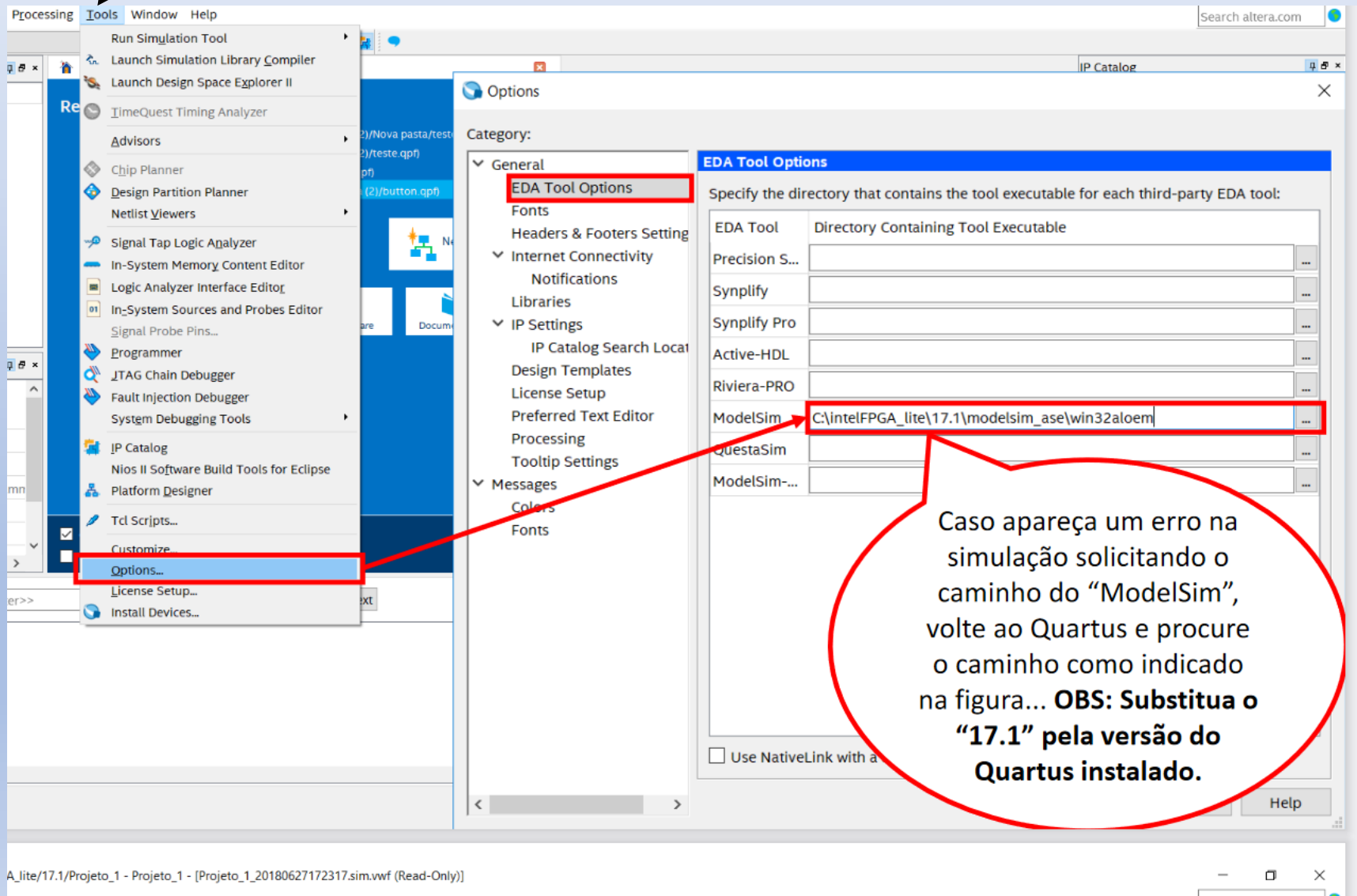

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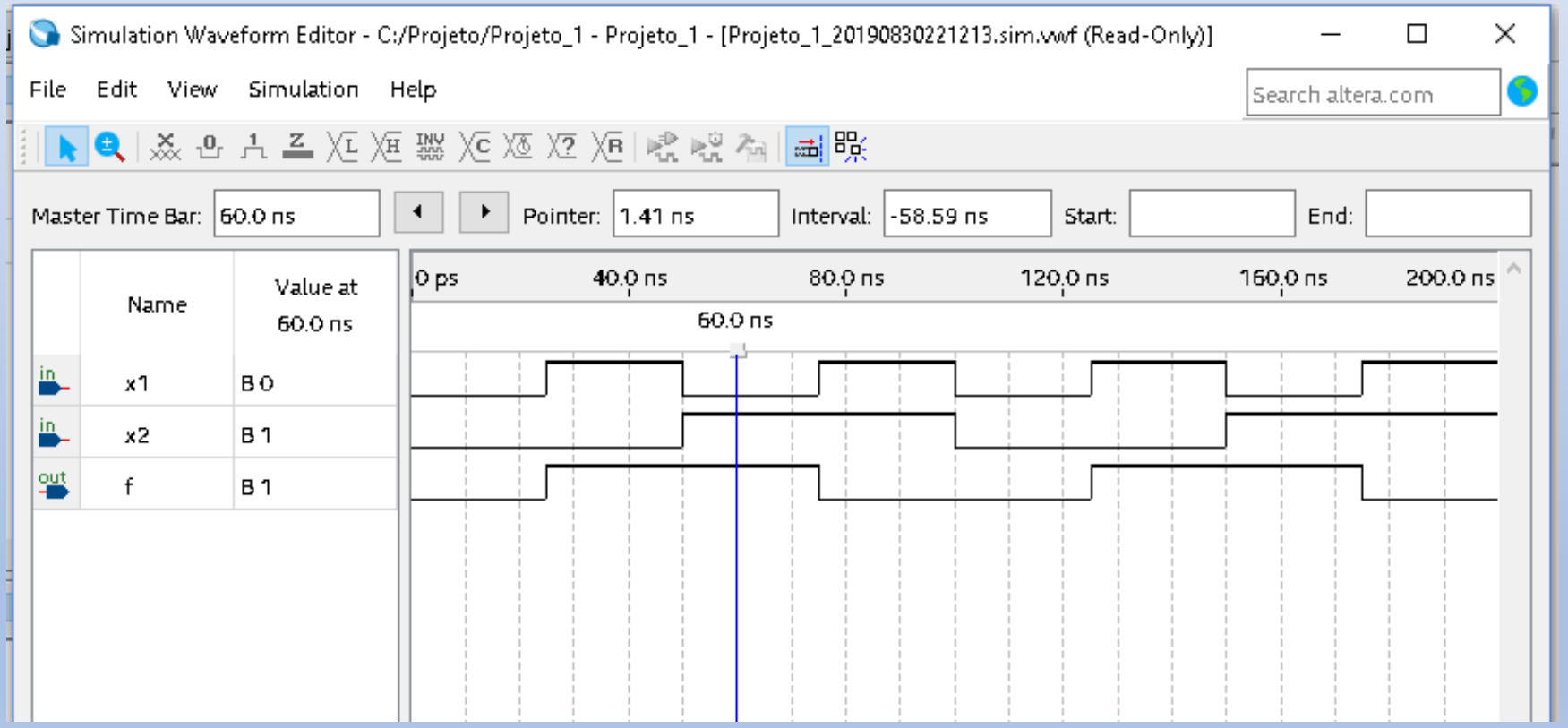
Salvar o Projeto_1 no diretorio C:/Projeto

Simulation – Run Functional Simulation



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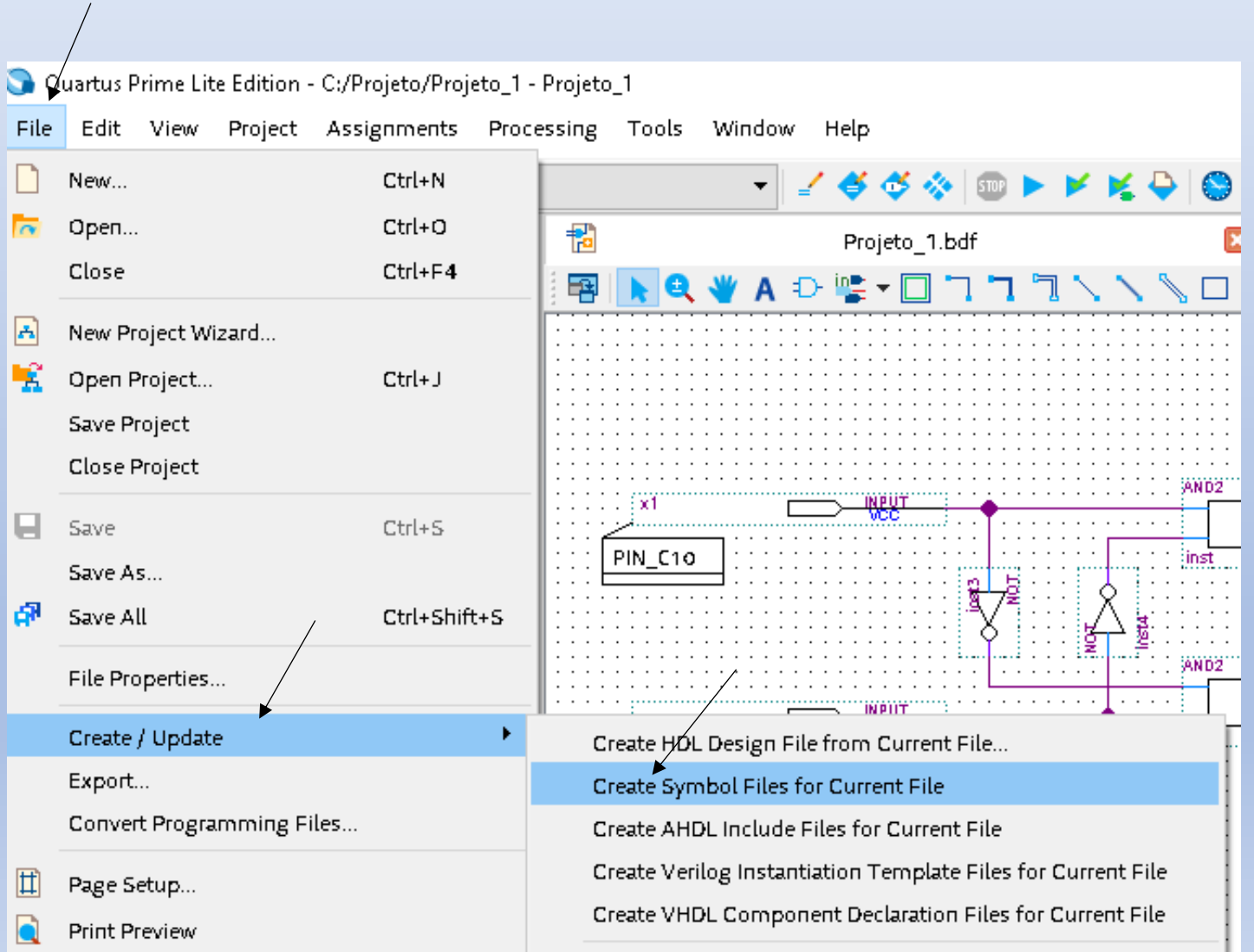
Criar um Simbolo Grafico

Na Tela do Editor Grafico :

File – Create/Update – Create Symbol Files for Current File



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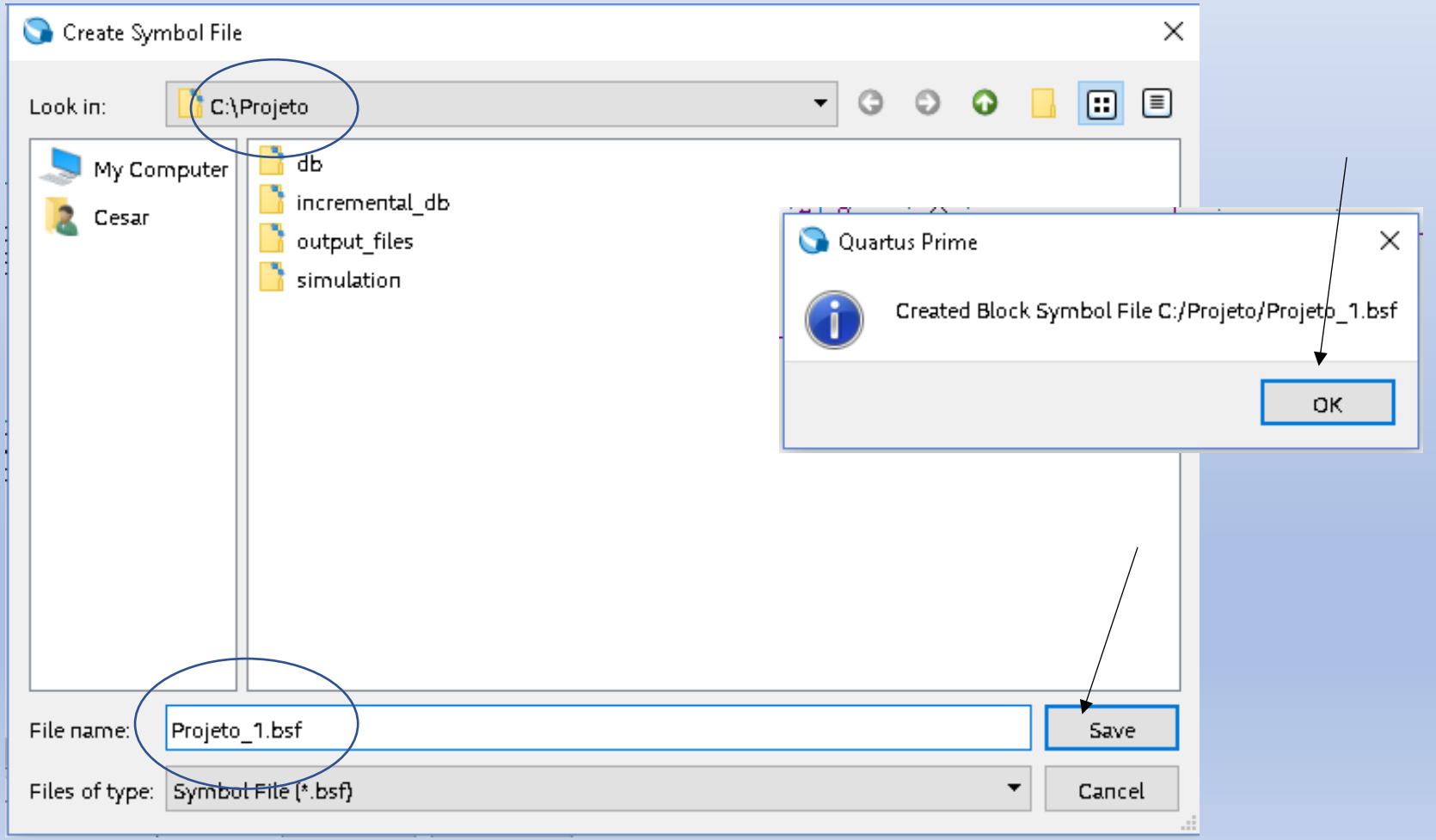
Criar um Simbolo Grafico

Salve o Arquivo - Ok



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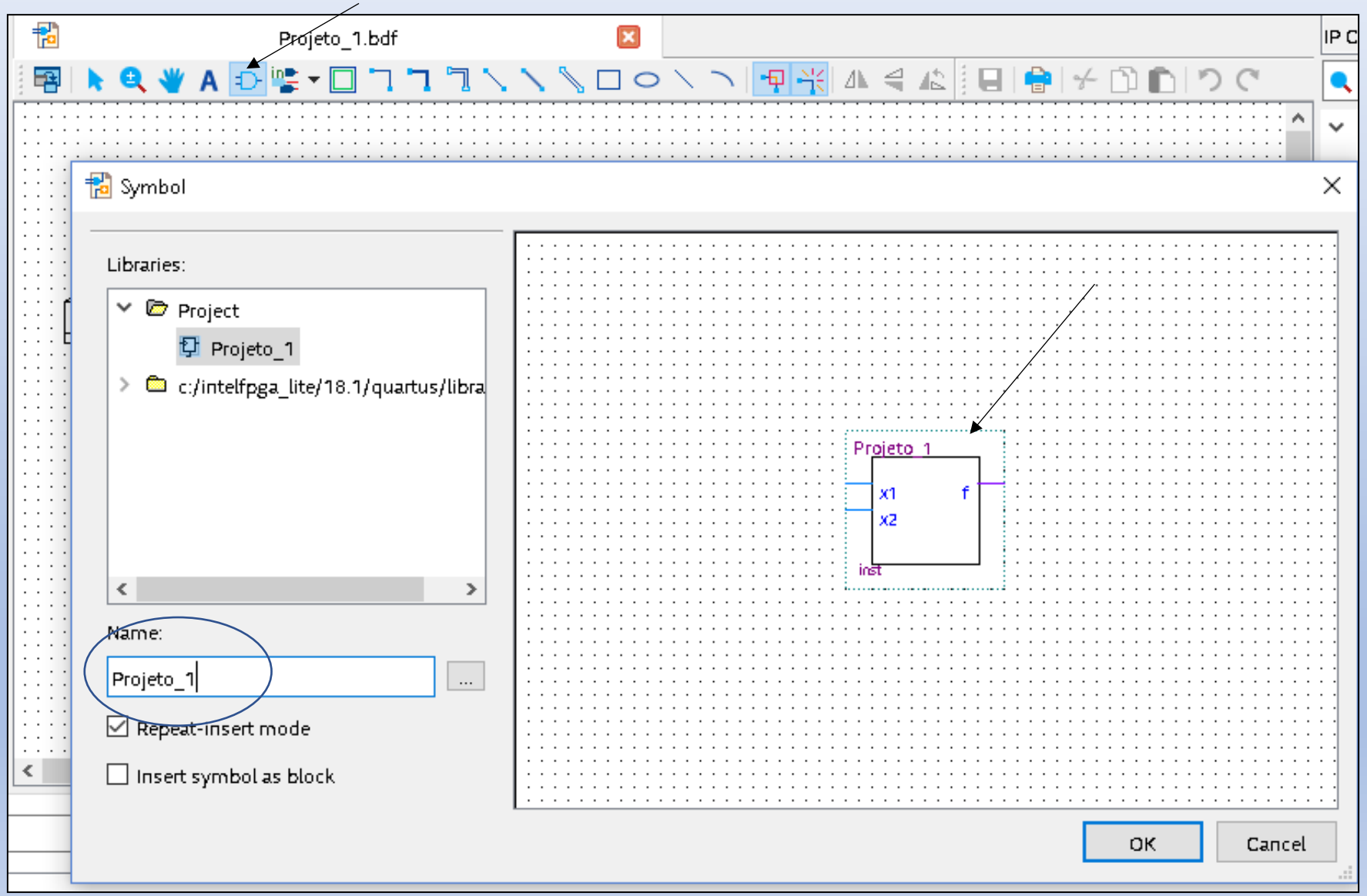
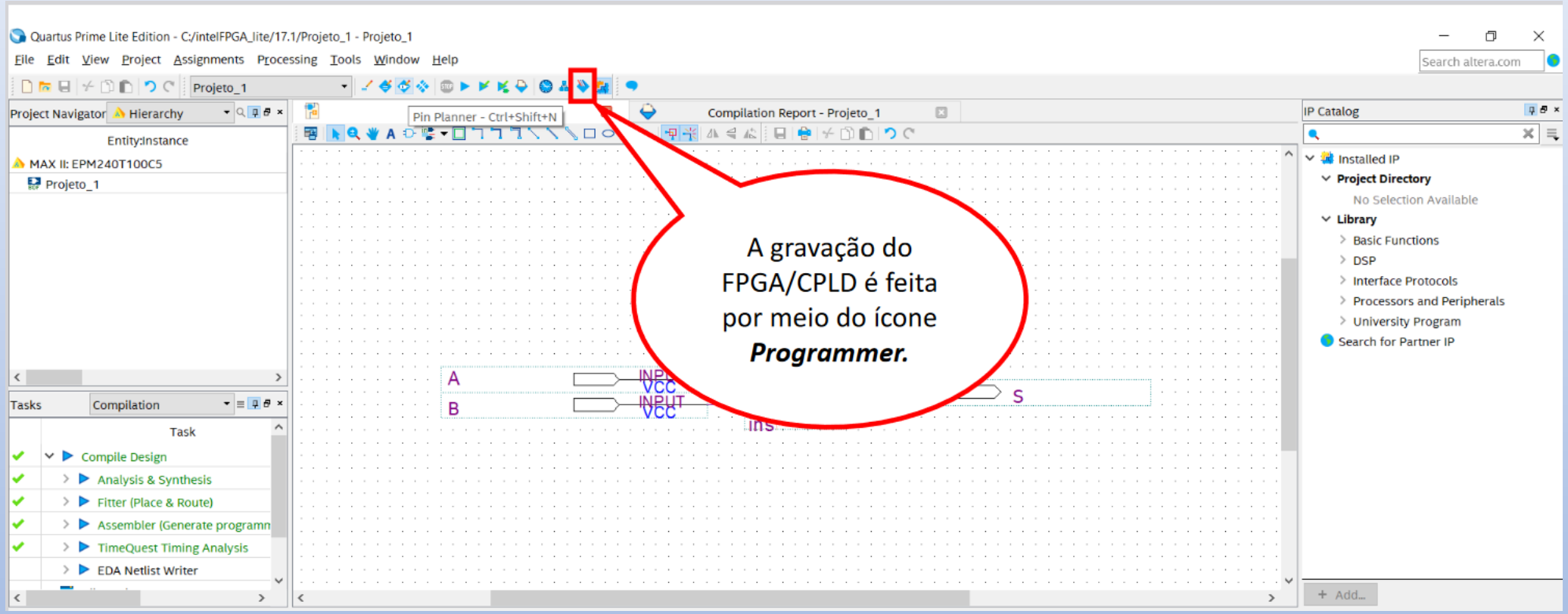
Selecione o Simbolo Grafico Criado



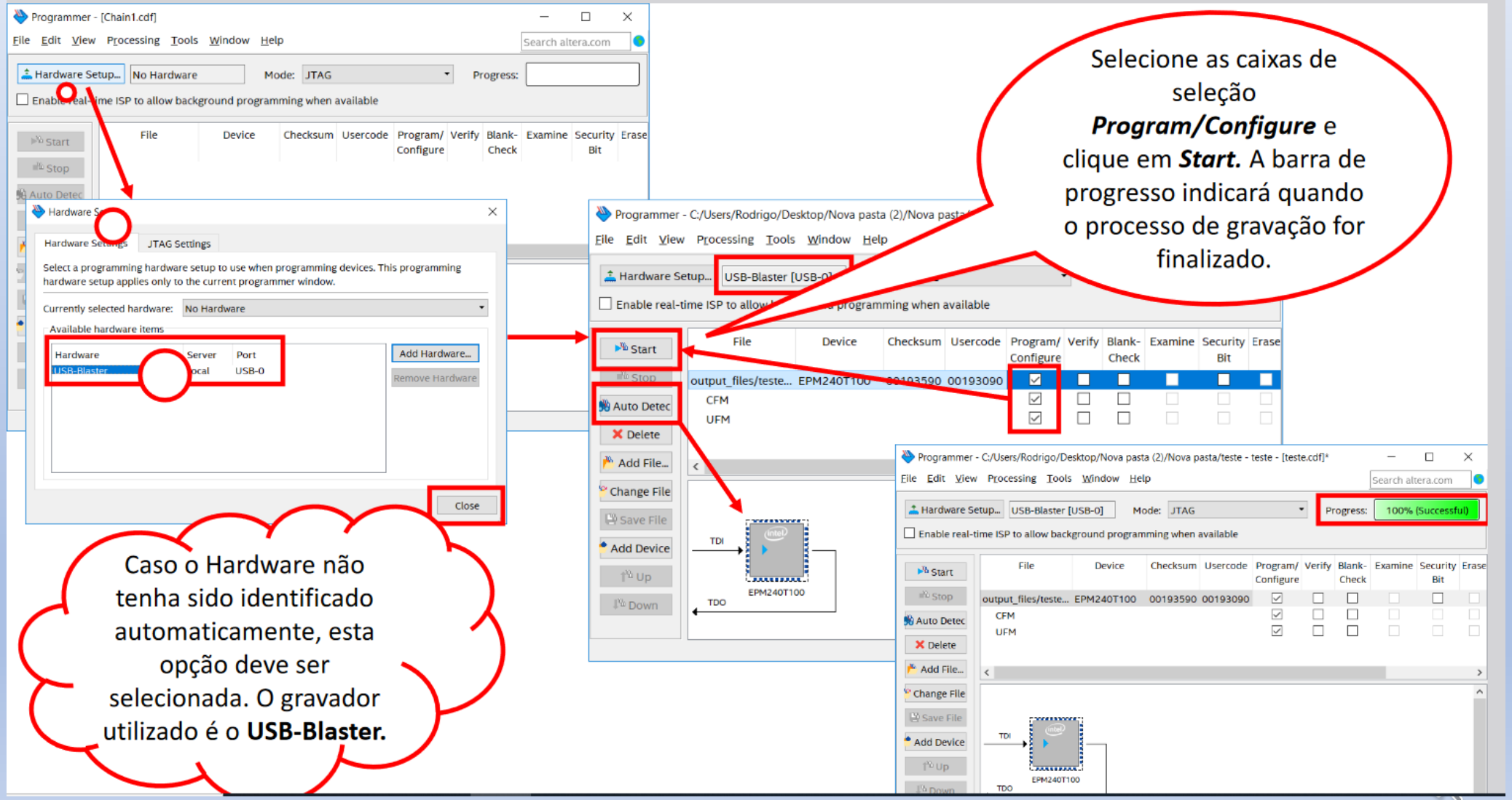
Descarregar o programa no Kit do FPGA

Menu – Tools - Programmer

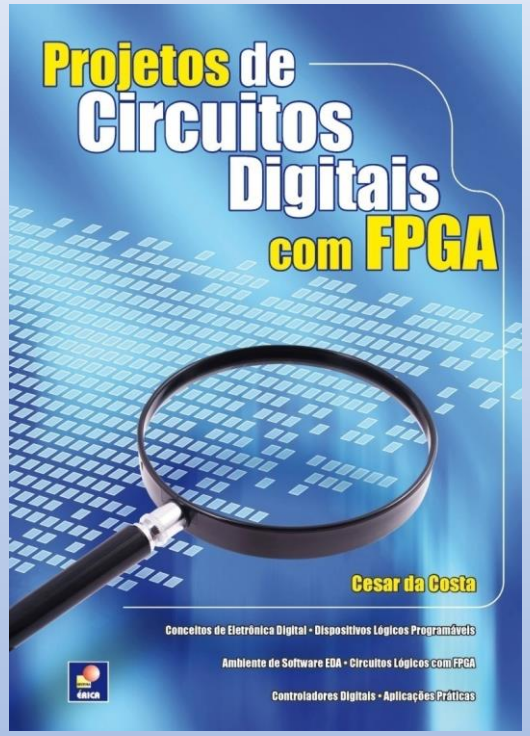


Descarregar o programa no Kit do FPGA

Menu – Tools - Programmer



Conclusões



Referência

https://www.youtube.com/watch?v=a2zQPHc4D9k

https://www.youtube.com/watch?v=X2QuGO-mrEY

Site www.professorcesarcosta.com.br

Tópicos:

-Disciplinas Ministradas T8LLC/LALOG;
- Kits Didáticos com FPGA;
- Clube do FPGA;
- FPGA;

Site www.fpgacentral.com

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