

# LABORATÓRIO DE LÓGICA CONFIGURÁVEL

Introdução ao Software Quartus Prime

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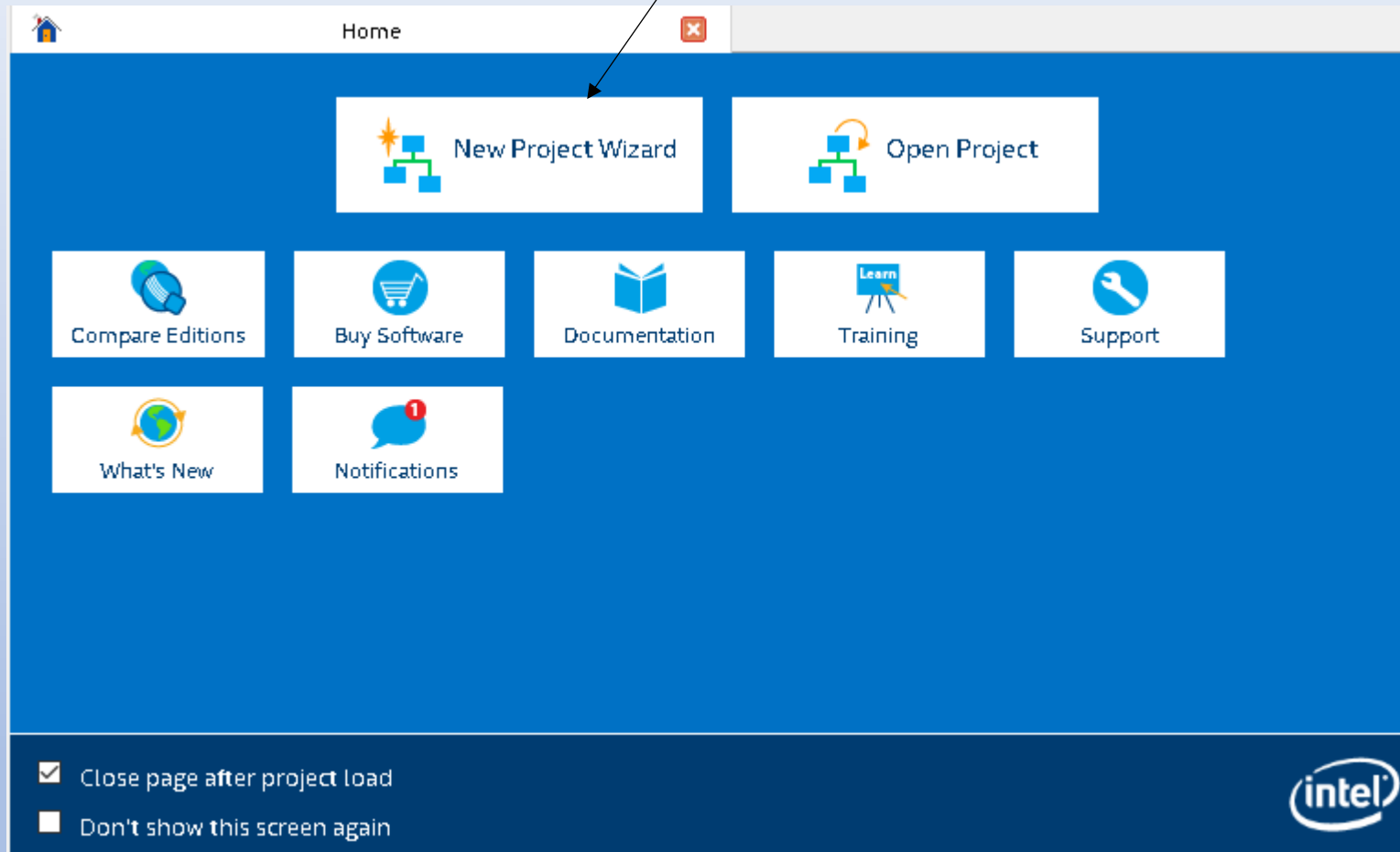
**Site: [www.professorcesarcosta.com.br](http://www.professorcesarcosta.com.br)**

# SOFTWARE QUARTUS PRIME Lite Edition



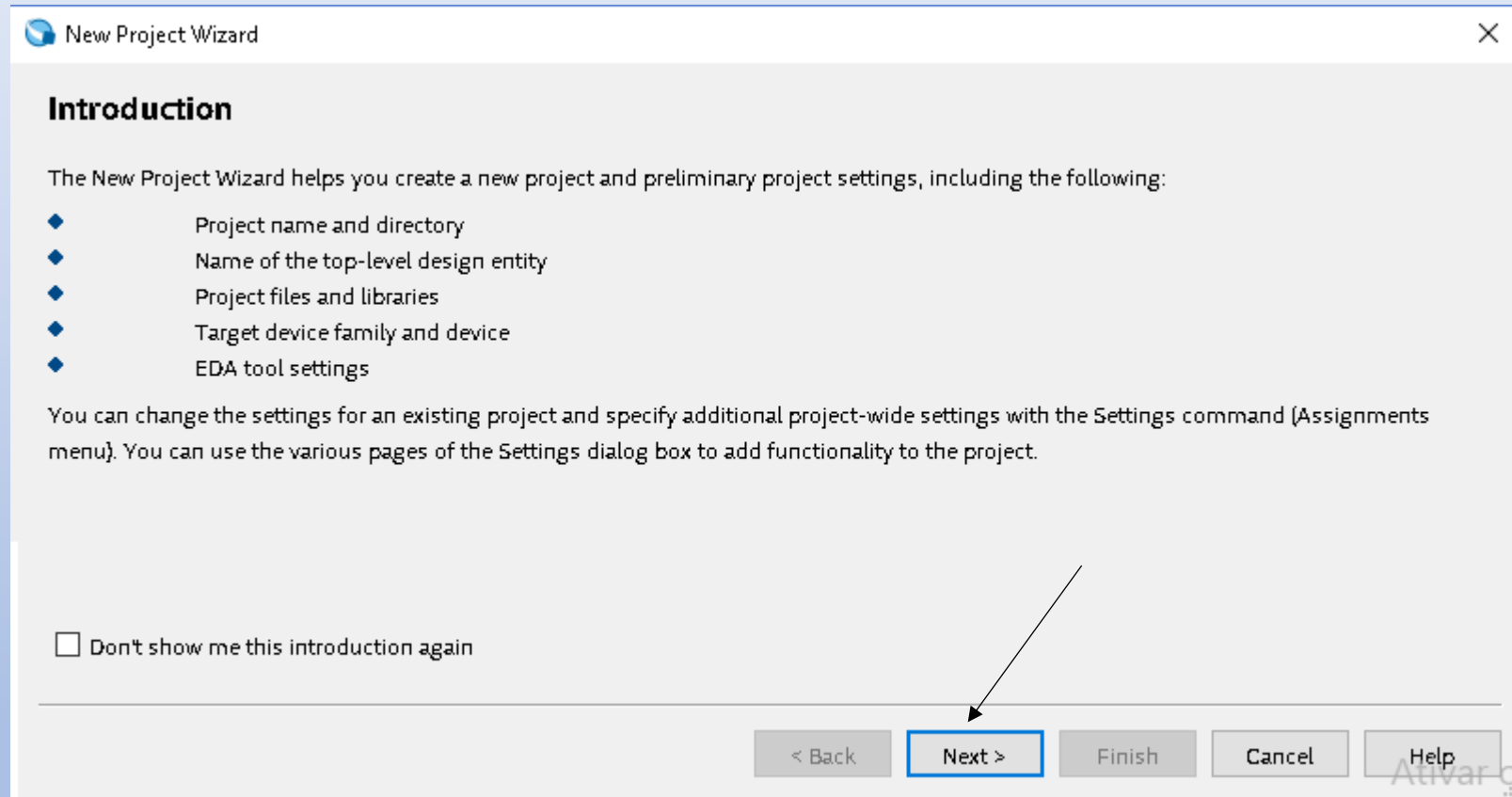
# SOFTWARE QUARTUS PRIME Lite Edition

File – New Project Wizard



# SOFTWARE QUARTUS PRIME Lite Edition

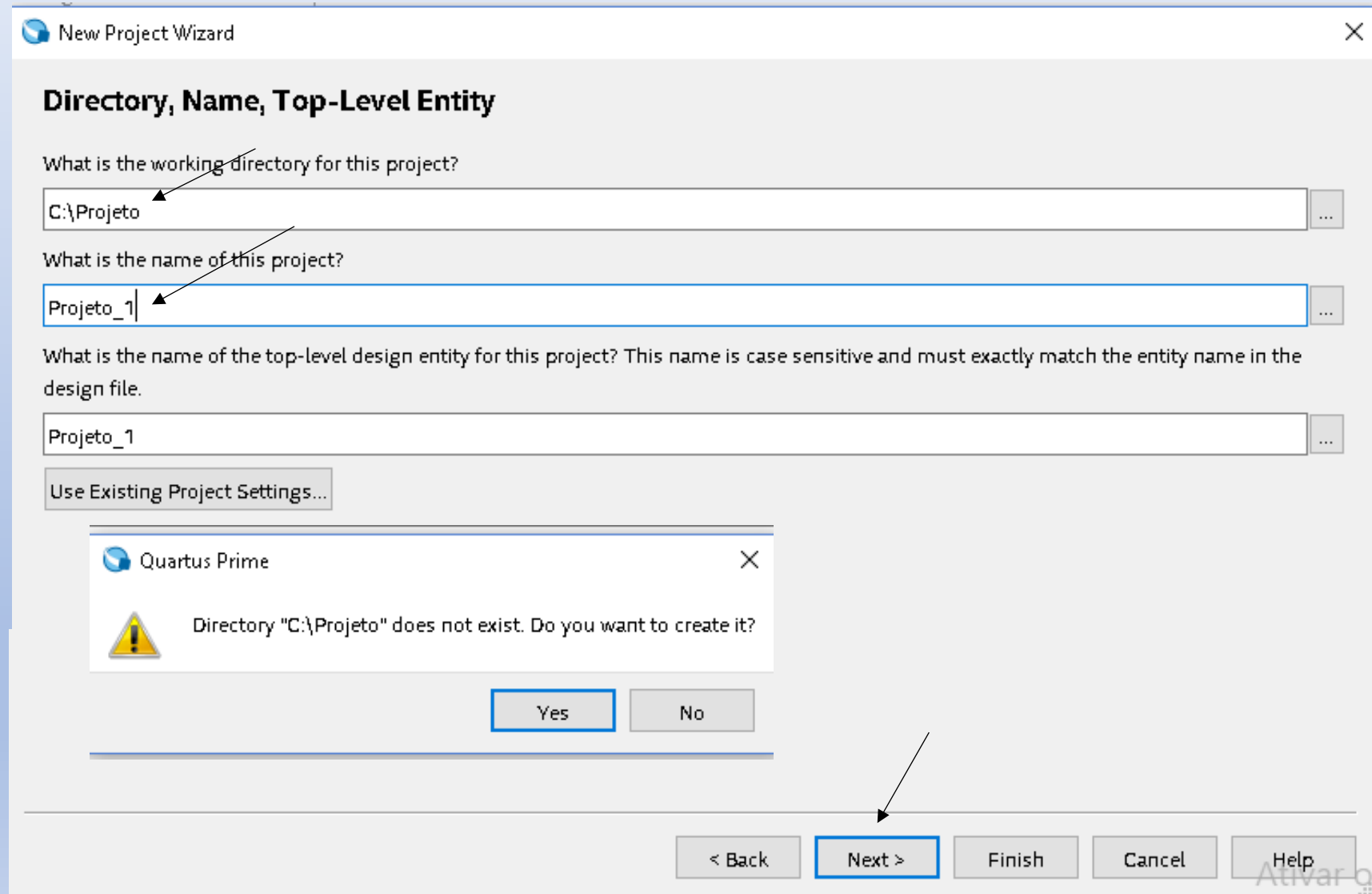
## 1. New Project ou Create a New Project



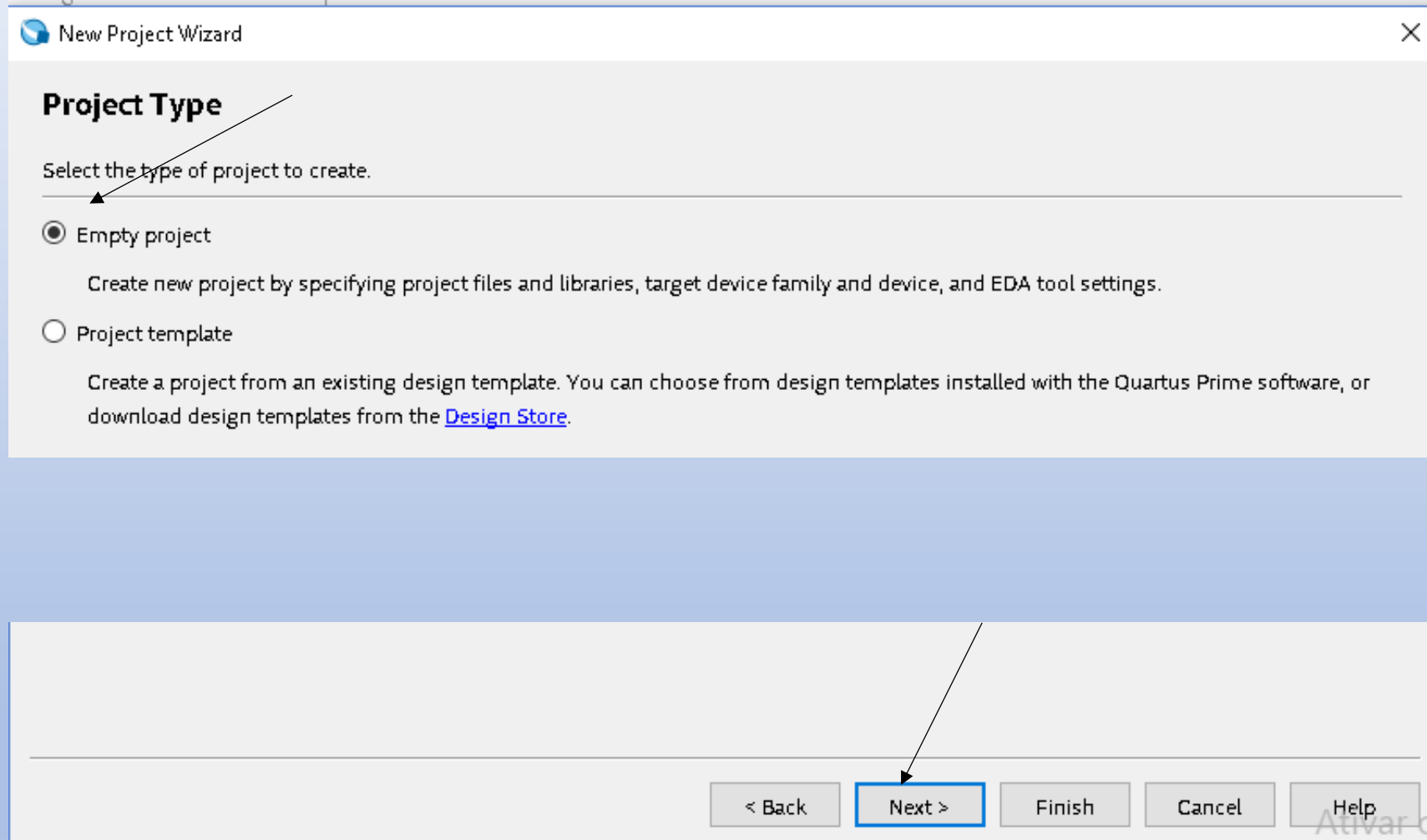


# SOFTWARE QUARTUS PRIME Lite Edition

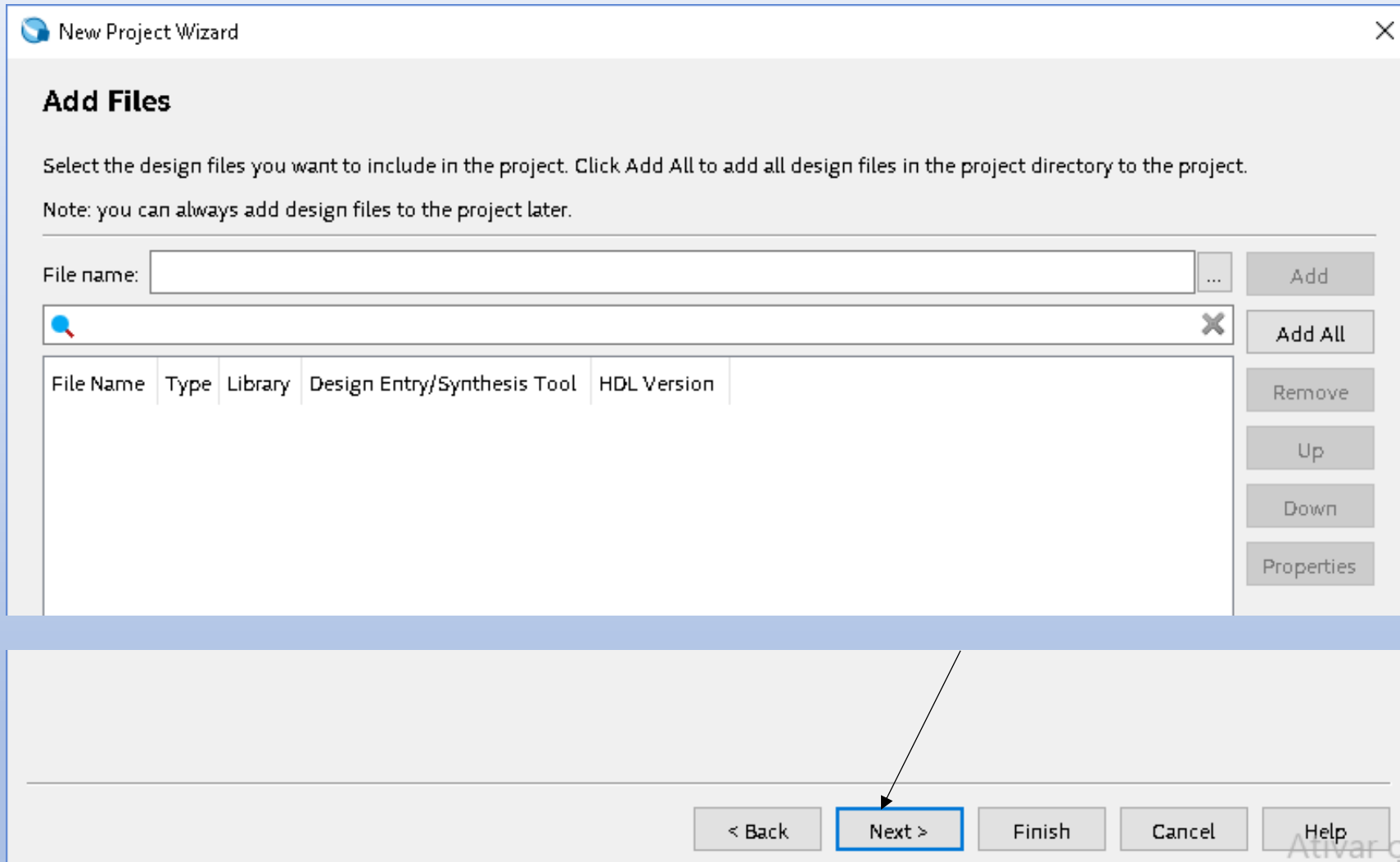
Criar o diretorio: Projeto e Nome do Projeto: Projeto\_1



# SOFTWARE QUARTUS PRIME Lite Edition



# SOFTWARE QUARTUS PRIME Lite Edition





# SOFTWARE QUARTUS PRIME Lite Edition

## Family, Device & Board Settings

Device Board

Select the family and device you want to target for compilation.

You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

**MAX 10**

Device family

Family: MAX 10 (DA/DF/DC/SA/SC)

Device: All

Show in 'Available devices' list

Package:

Any

Pin count:

Any

Core speed grade:

Any

Name filter:

Show advanced devices

Target device

Auto device selected by the Fitter

Specific device selected in 'Available devices' list

Other: n/a

Available devices:

Name	Core Voltage	LEs	Total I/Os	GPIOs	Memory Bits	Embedded multiplier
10M50DAF484C7G	1.2V	49760	360	360	1677312	288

**10M50DAF484C7G**

< Back

Next >

Finish

Cancel

Help

# SOFTWARE QUARTUS PRIME Lite Edition

New Project Wizard

## EDA Tool Settings

Specify the other EDA tools used with the Quartus Prime software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synth...	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	<None>	<None>	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

< Back   **Next >**   Finish   Cancel   Help

# SOFTWARE QUARTUS PRIME Lite Edition

New Project Wizard

## Summary

When you click Finish, the project will be created with the following settings:

Project directory:	C:\Projeto
Project name:	Projeto_1
Top-level design entity:	Projeto_1
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Design template:	n/a
Family name:	MAX 10 (DA/DF/DC/SA/SC)
Device:	10M08DAF484C8G
Board:	n/a
EDA tools:	
Design entry/synthesis:	<None> [<None>]
Simulation:	<None> [<None>]
Timing analysis:	0
Operating conditions:	
Core voltage:	1.2V
Junction temperature range:	0-85 °C

< Back    Next >    **Finish**    Cancel    Help

# SOFTWARE QUARTUS PRIME Lite Edition

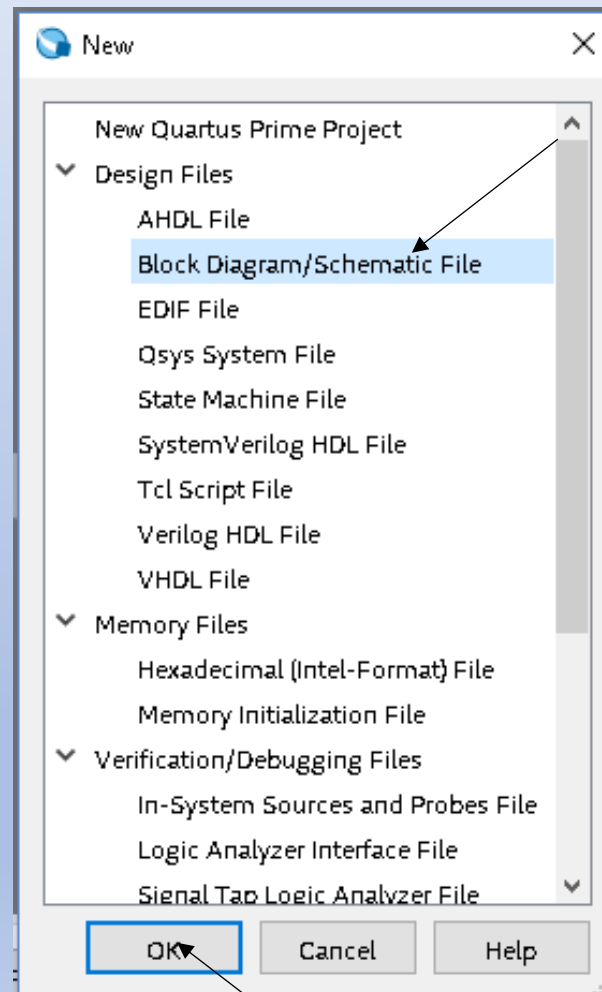
A tela indica que o projeto foi criado.

The screenshot displays the Quartus Prime software interface. The main window shows the 'Quartus Prime' logo and 'Version 18.1 Lite Edition'. On the left, the 'Entity:Instance' pane shows a project named 'Projeto\_1' under the device 'MAX 10: 10M08DAF484C8G'. The 'Tasks' pane is set to 'Compilation' and lists tasks such as 'Compile Design', 'Analysis & Synthesis', 'Fitter (Place & Route)', 'Assembler (Generate programr', and 'Timine Analysis'. At the bottom, a message pane displays the following information:

Type	ID	Message
	253020	Default device 10M08DAF484C8G is automatically selected for the device family MAX 10

# SOFTWARE QUARTUS PRIME Lite Edition

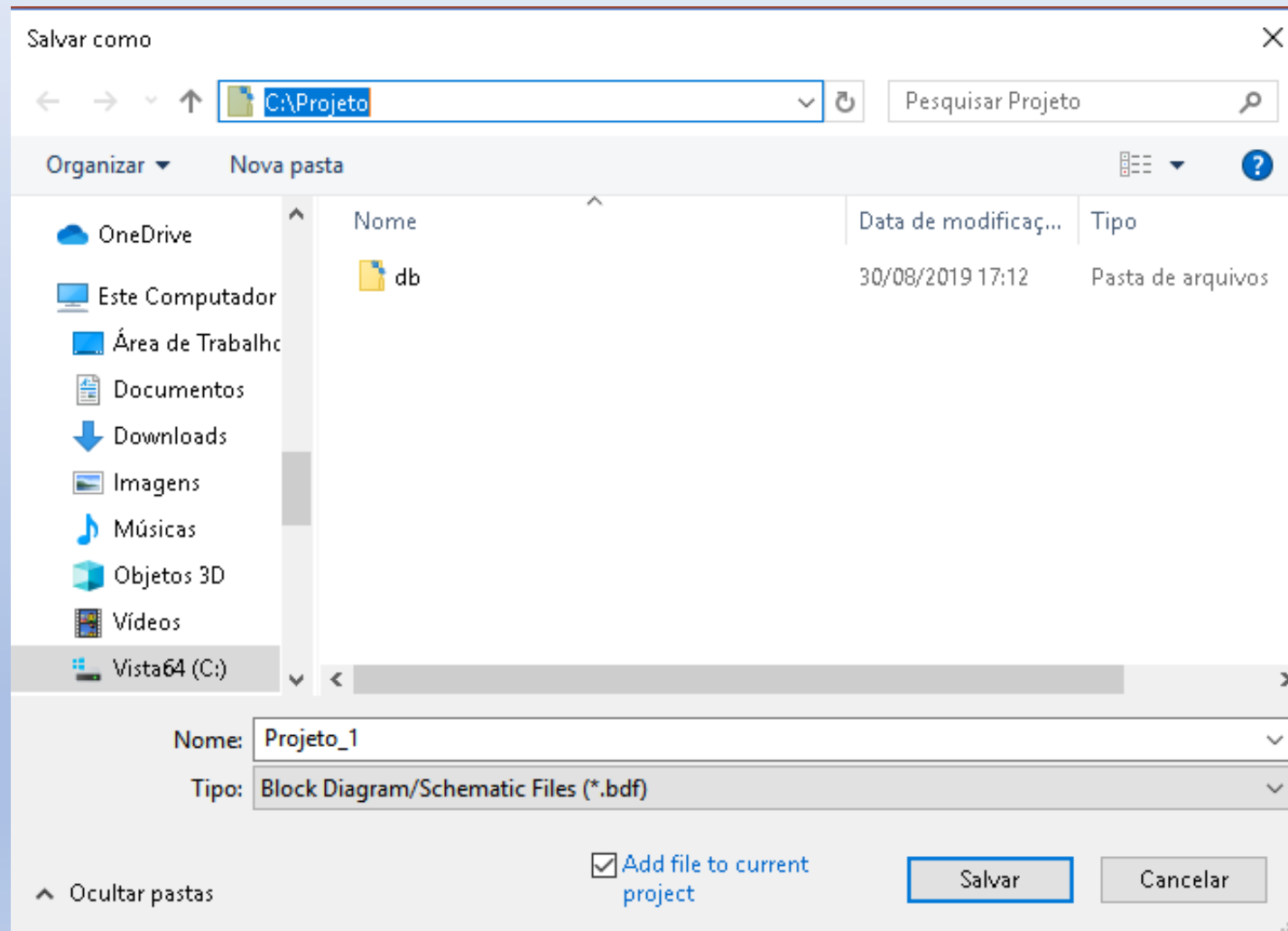
File – New – Block Diagram/Schematic File



# SOFTWARE QUARTUS PRIME Lite Edition

Editor Grafico

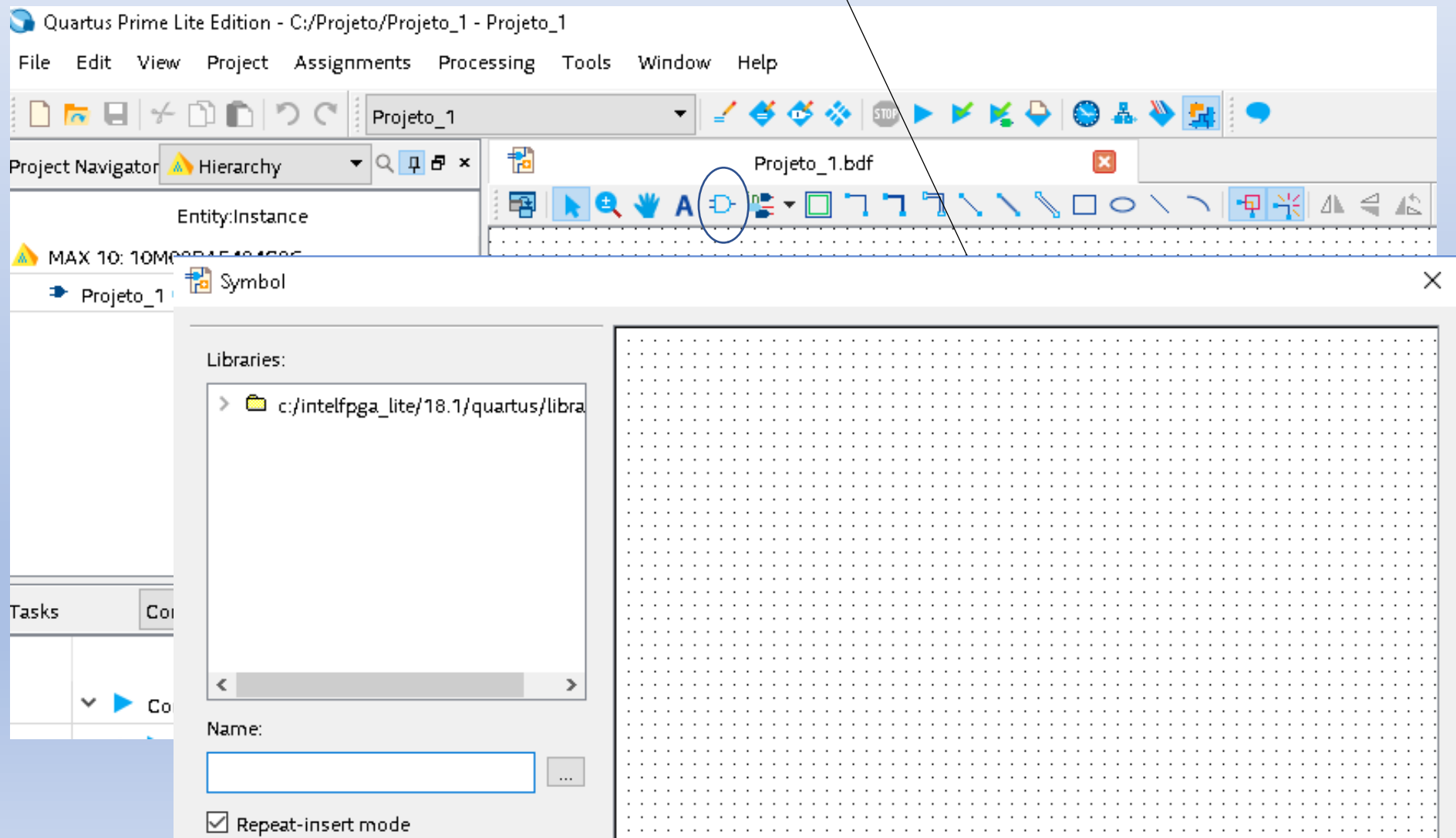
File – Save As – Projeto\_1 (Pasta Projeto)



# SOFTWARE QUARTUS PRIME Lite Edition

## Editor Grafico

- 2 clicks no meio da tela de trabalho surge a tela symbol



# SOFTWARE QUARTUS PRIME Lite Edition

## Exercicio 1:

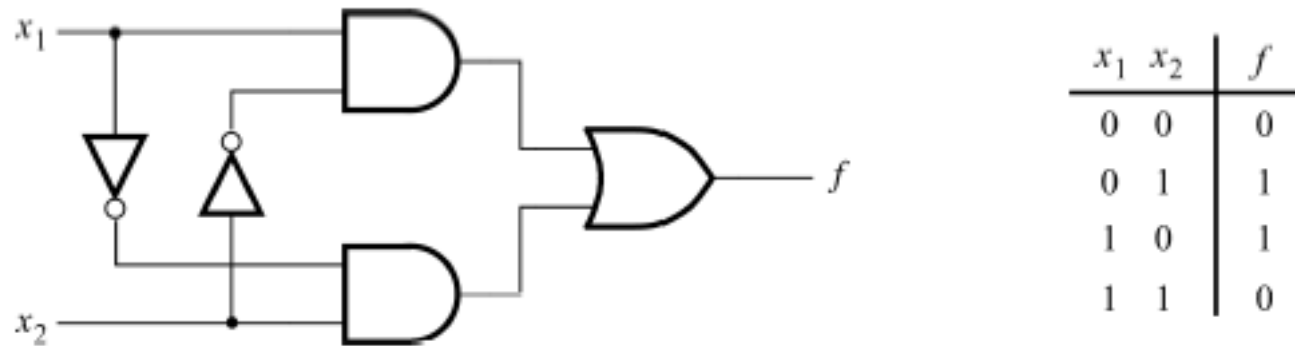
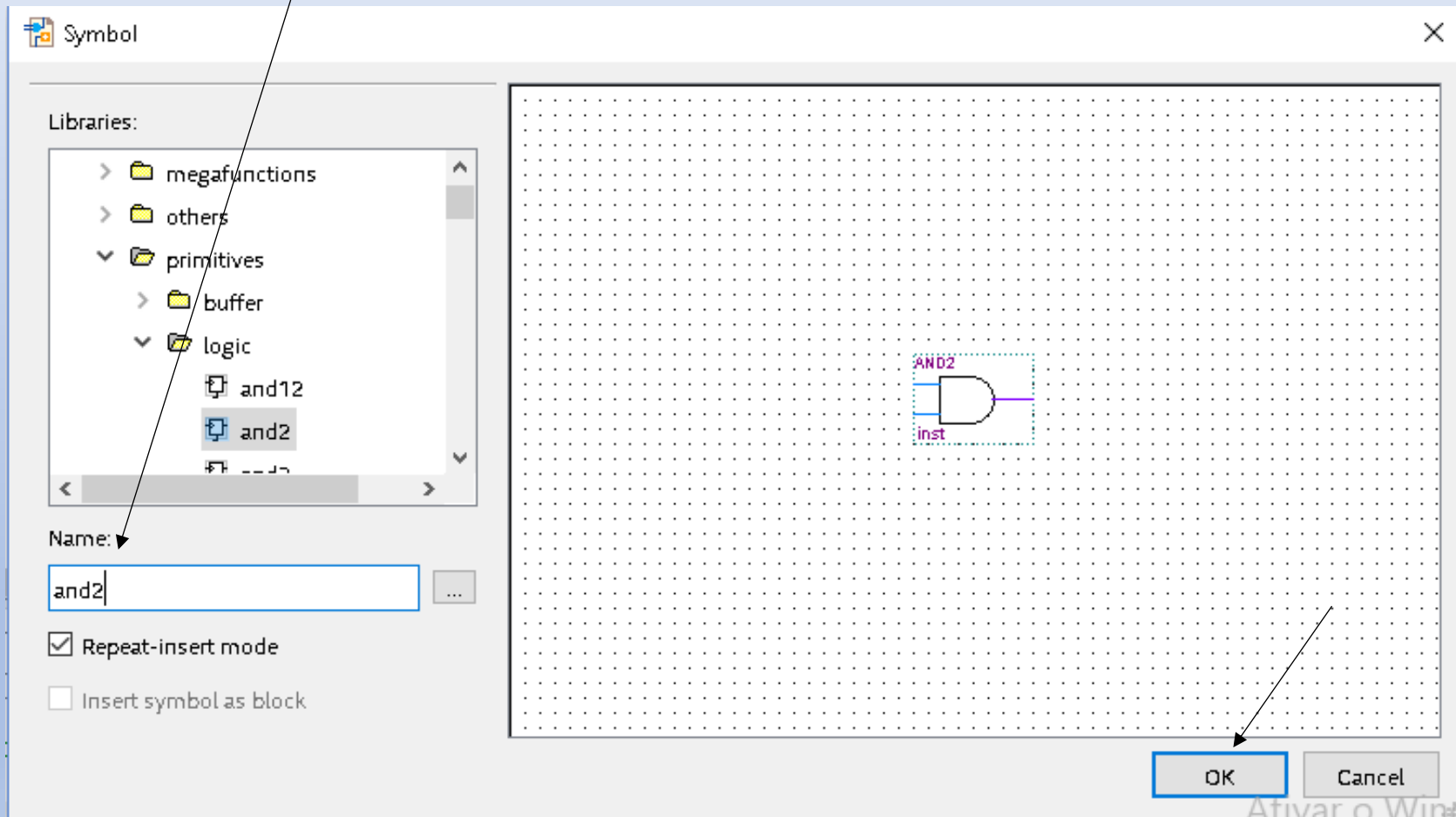


Figure 12. The light controller circuit.



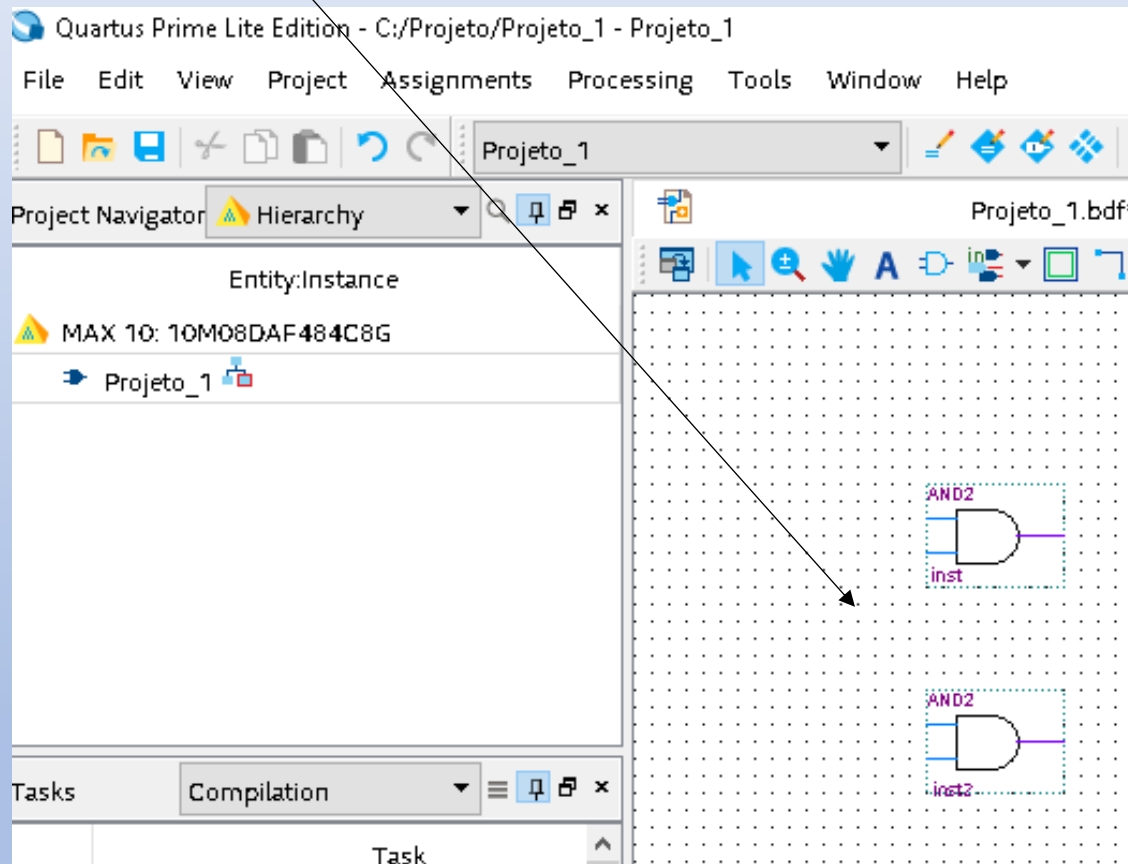
# SOFTWARE QUARTUS PRIME Lite Edition

Inserir os componentes desejados



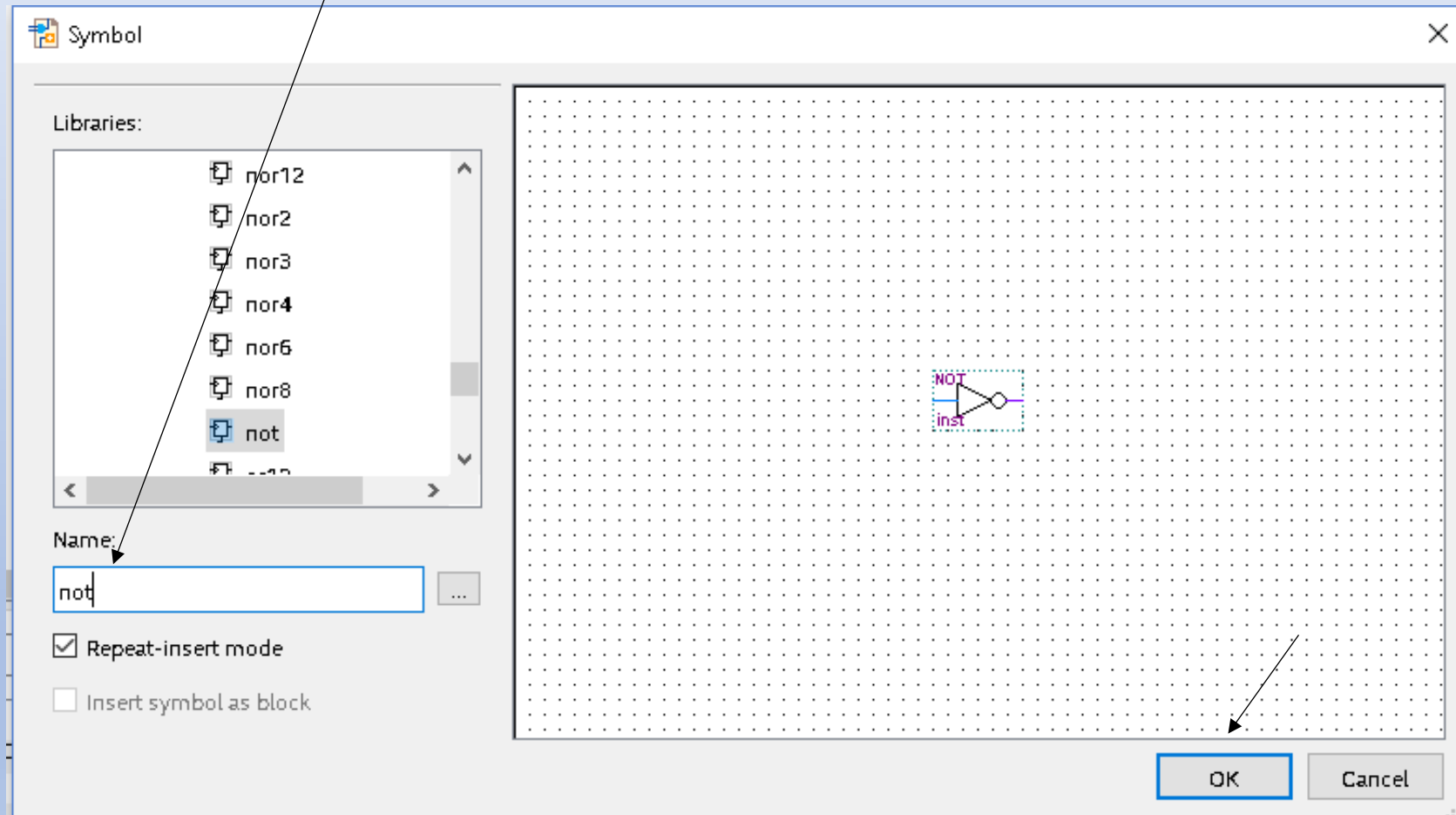
# SOFTWARE QUARTUS PRIME Lite Edition

Inserir 2 portas AND



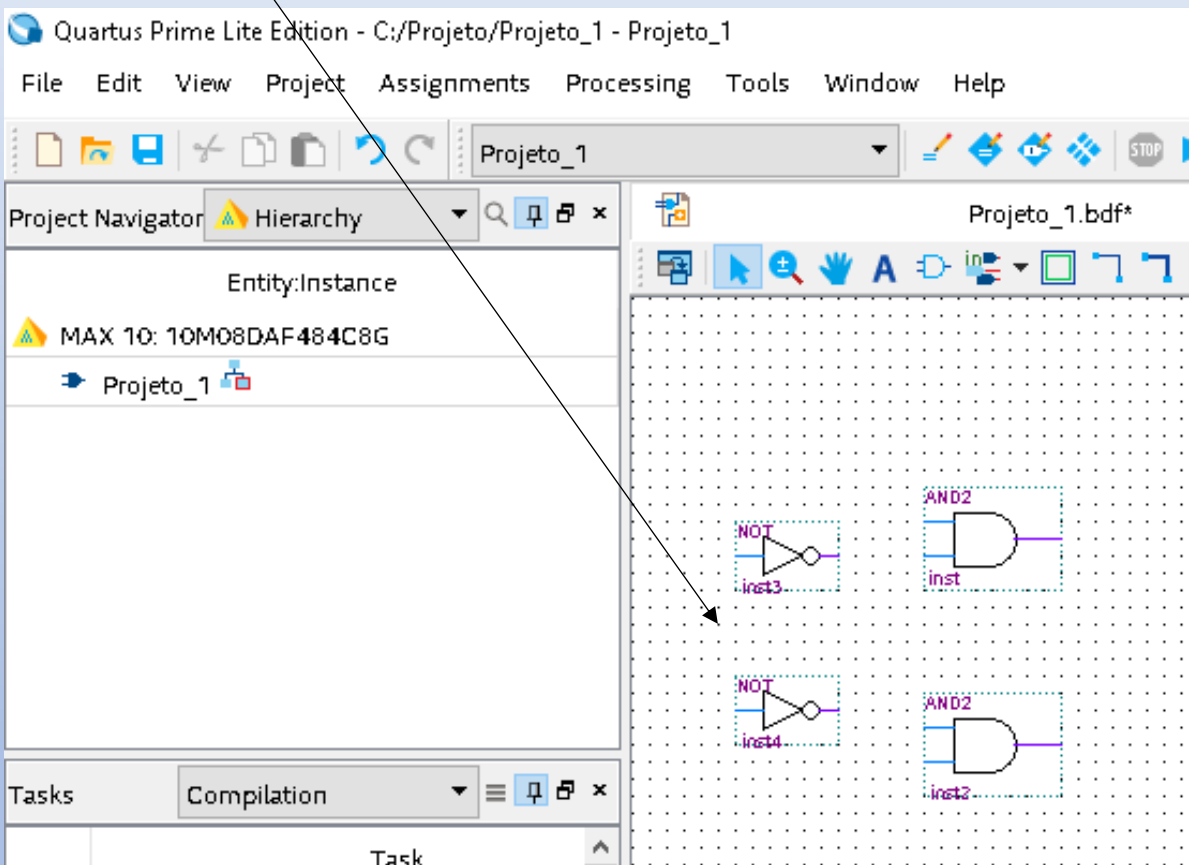
# SOFTWARE QUARTUS PRIME Lite Edition

Seleziona la porta NOT



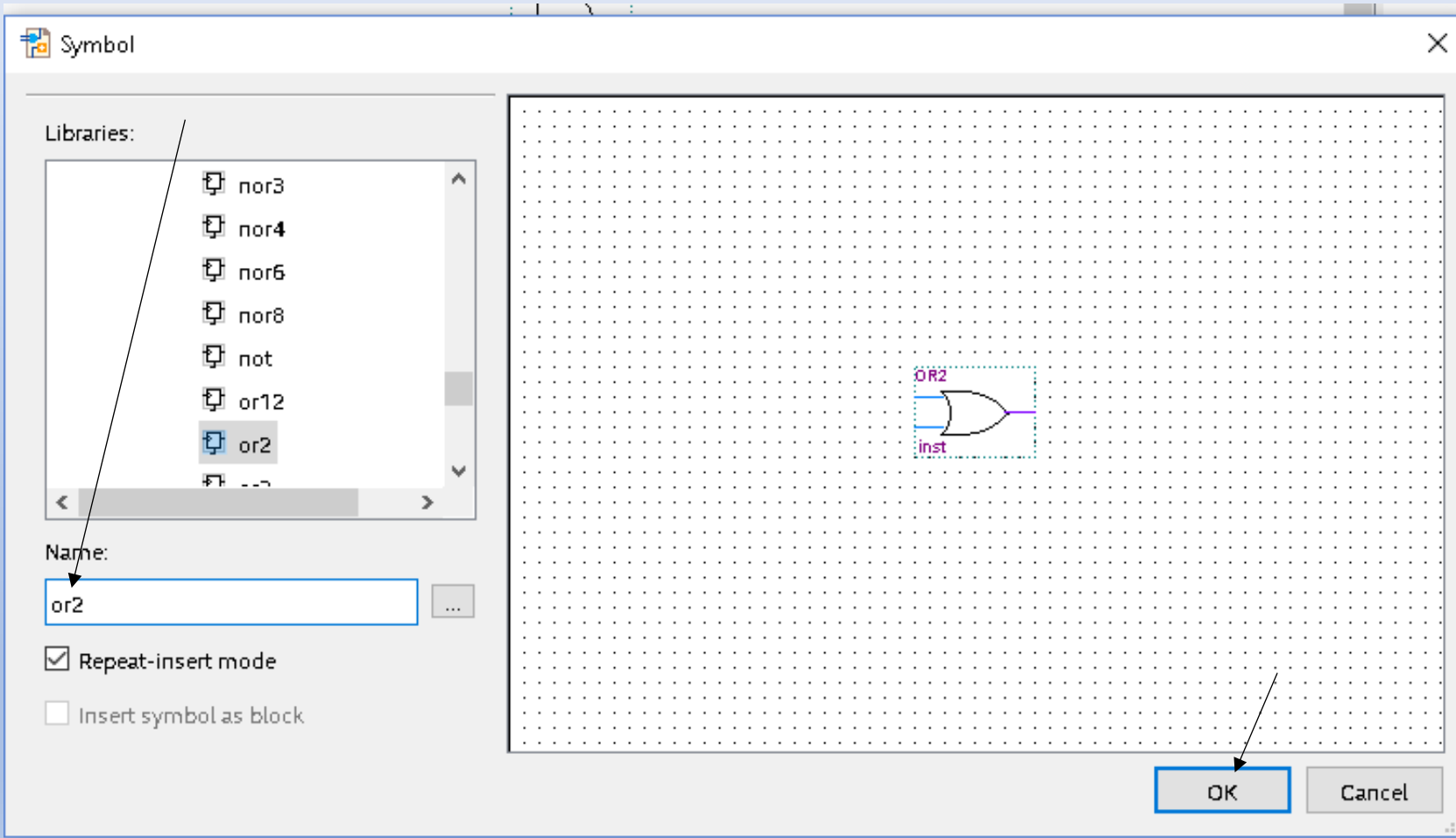
# SOFTWARE QUARTUS PRIME Lite Edition

Posicione as duas portas NOT



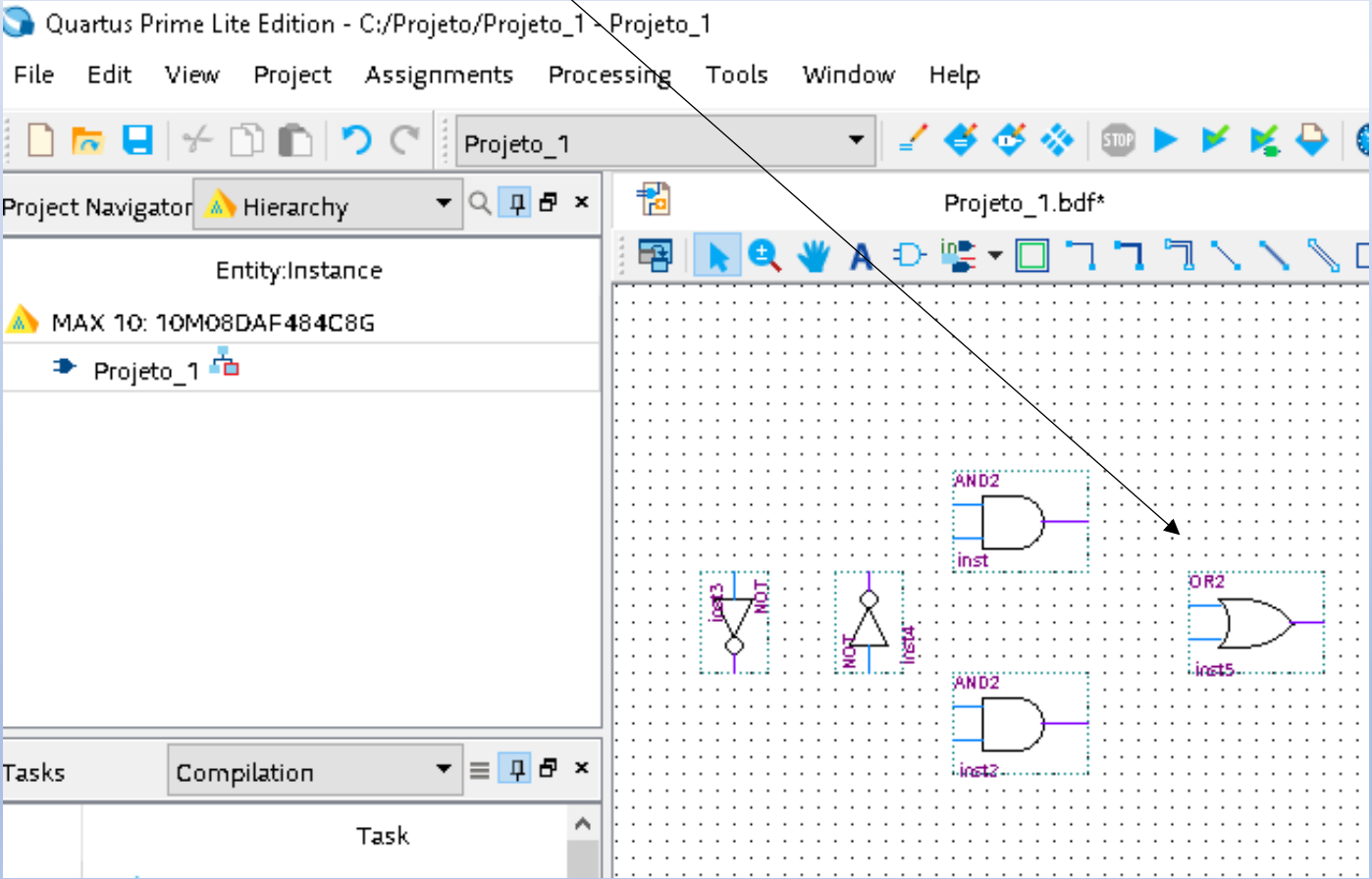
# SOFTWARE QUARTUS PRIME Lite Edition

Selecione a porta OR



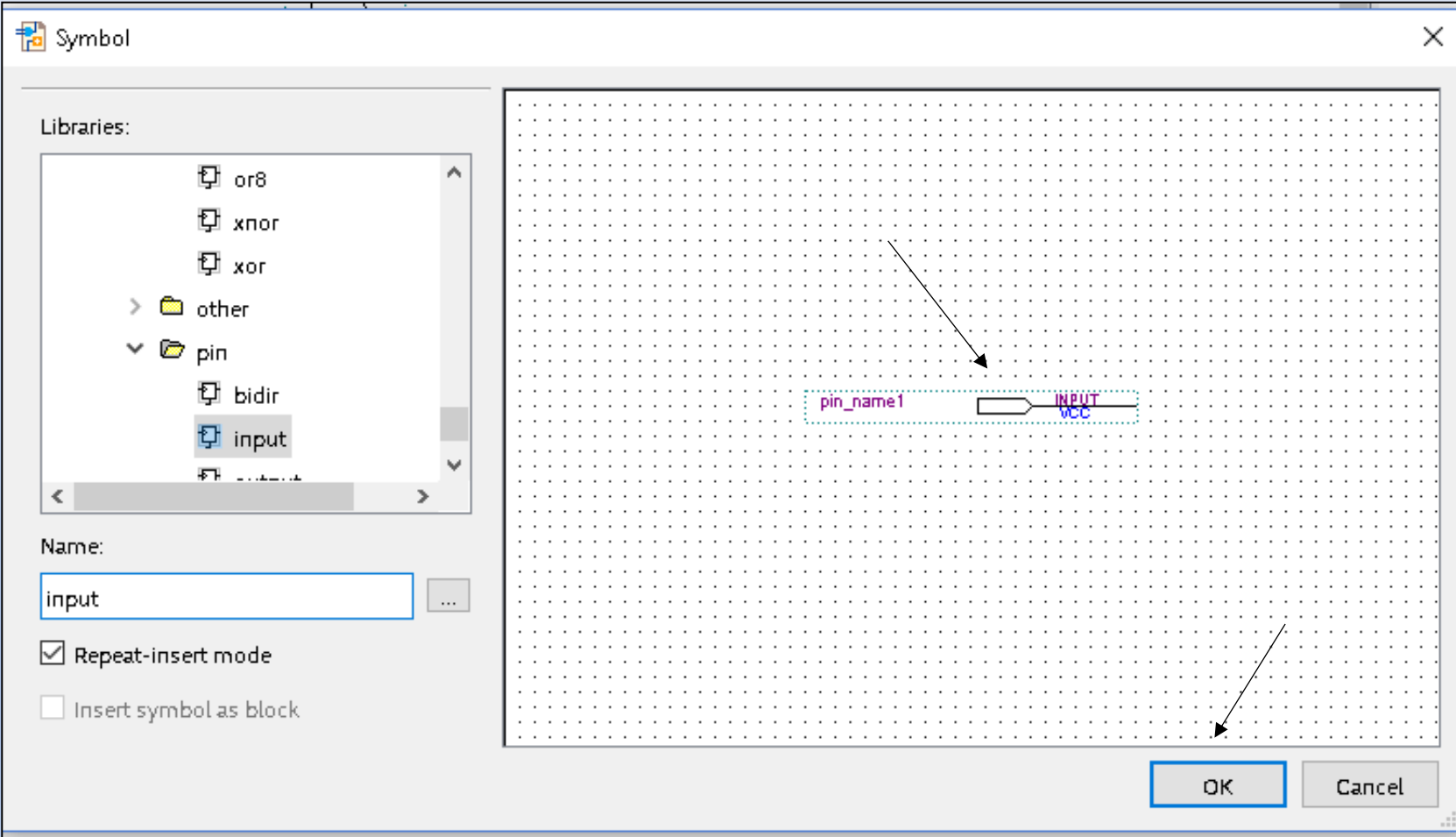
# SOFTWARE QUARTUS PRIME Lite Edition

Posicione a porta OR



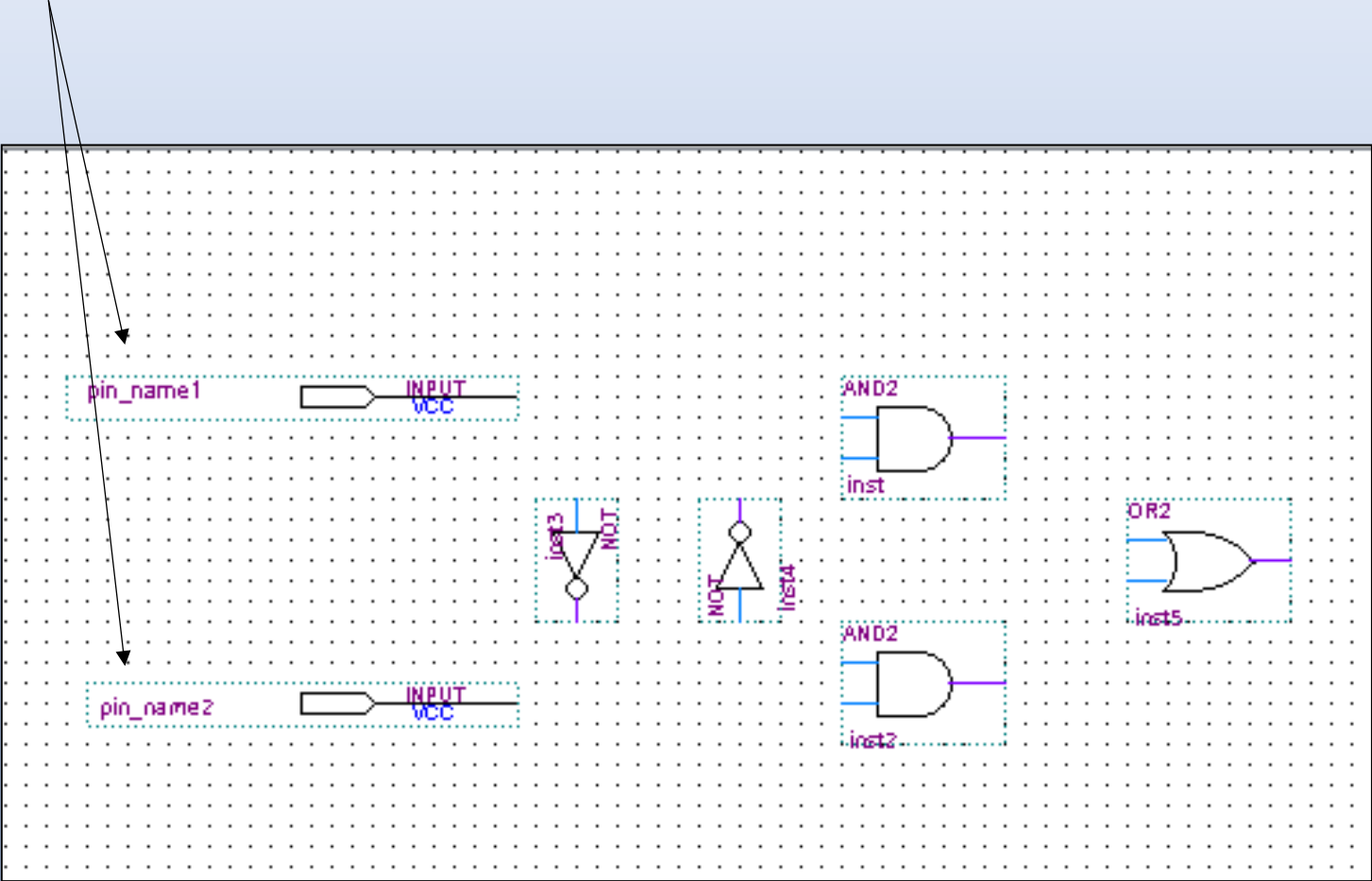
# SOFTWARE QUARTUS PRIME Lite Edition

Inserir terminais de entrada



# SOFTWARE QUARTUS PRIME Lite Edition

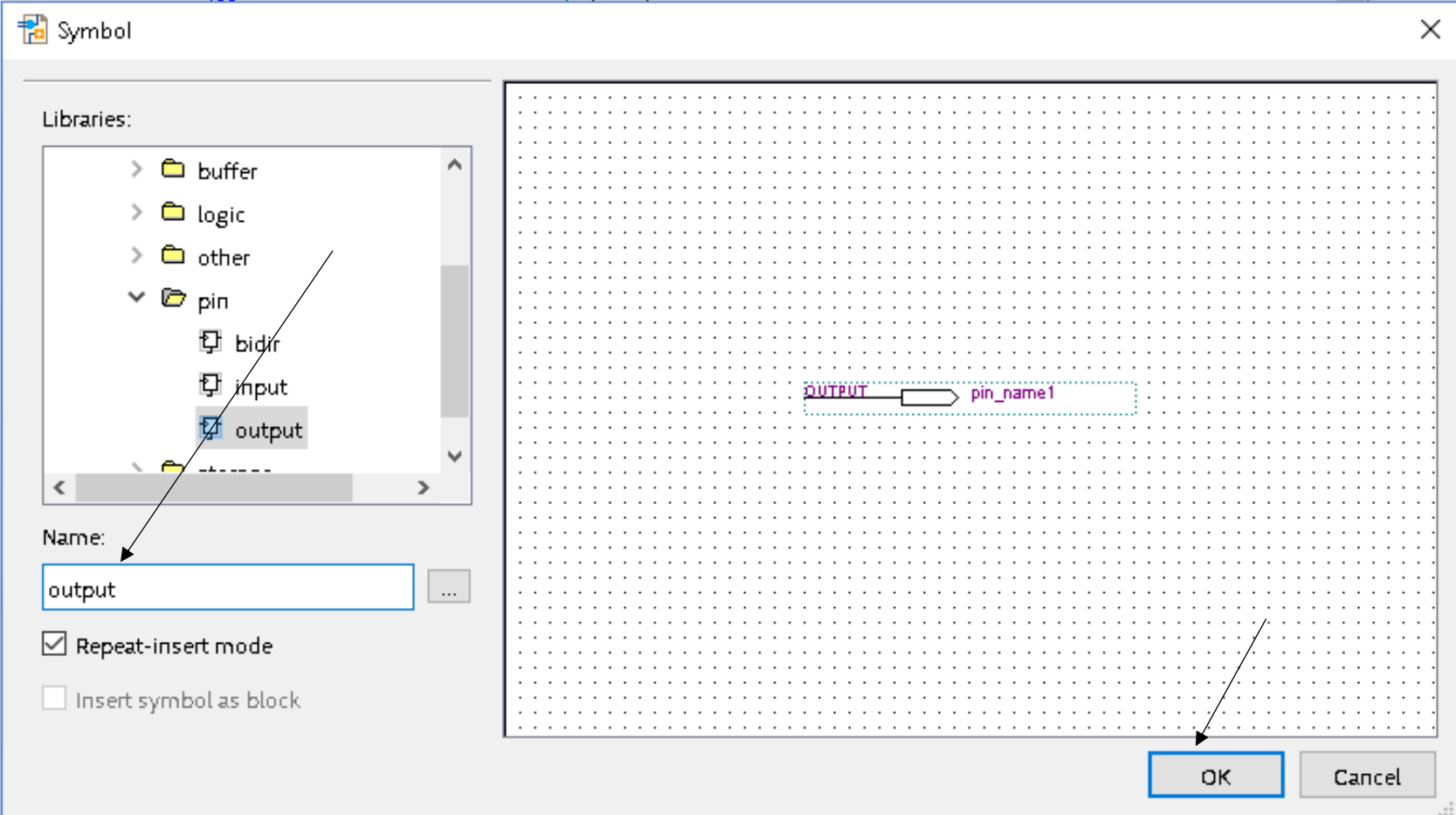
Posicione os 2 terminais de entrada





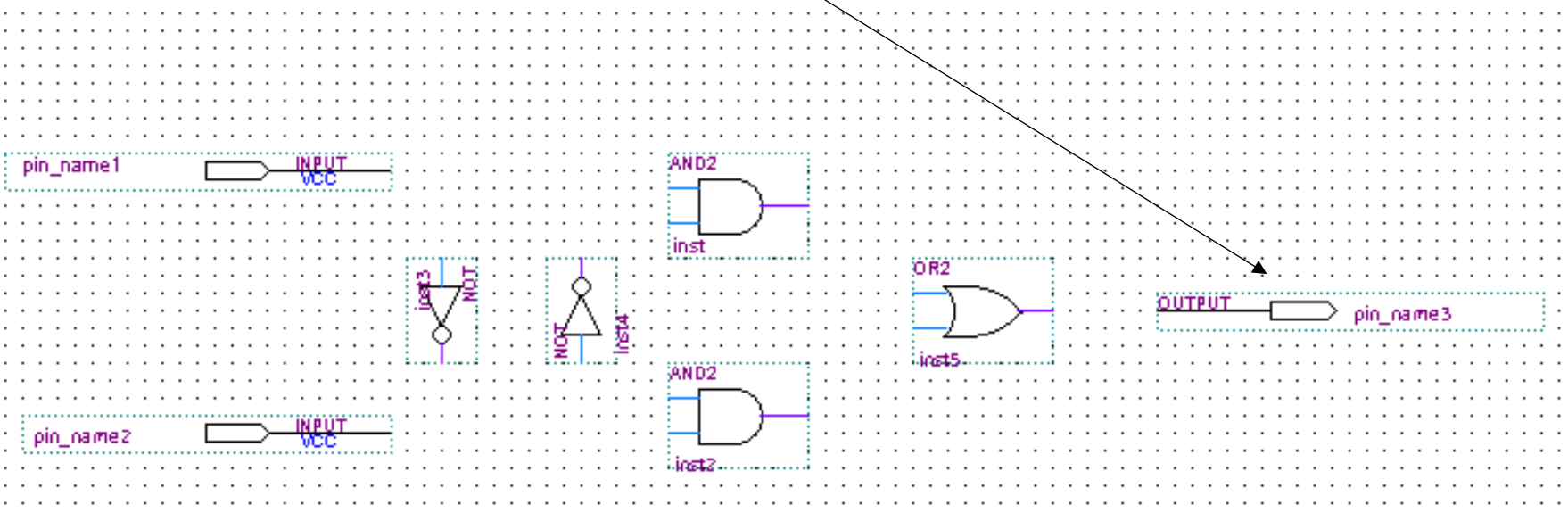
# SOFTWARE QUARTUS PRIME Lite Edition

Inserir terminal de saida



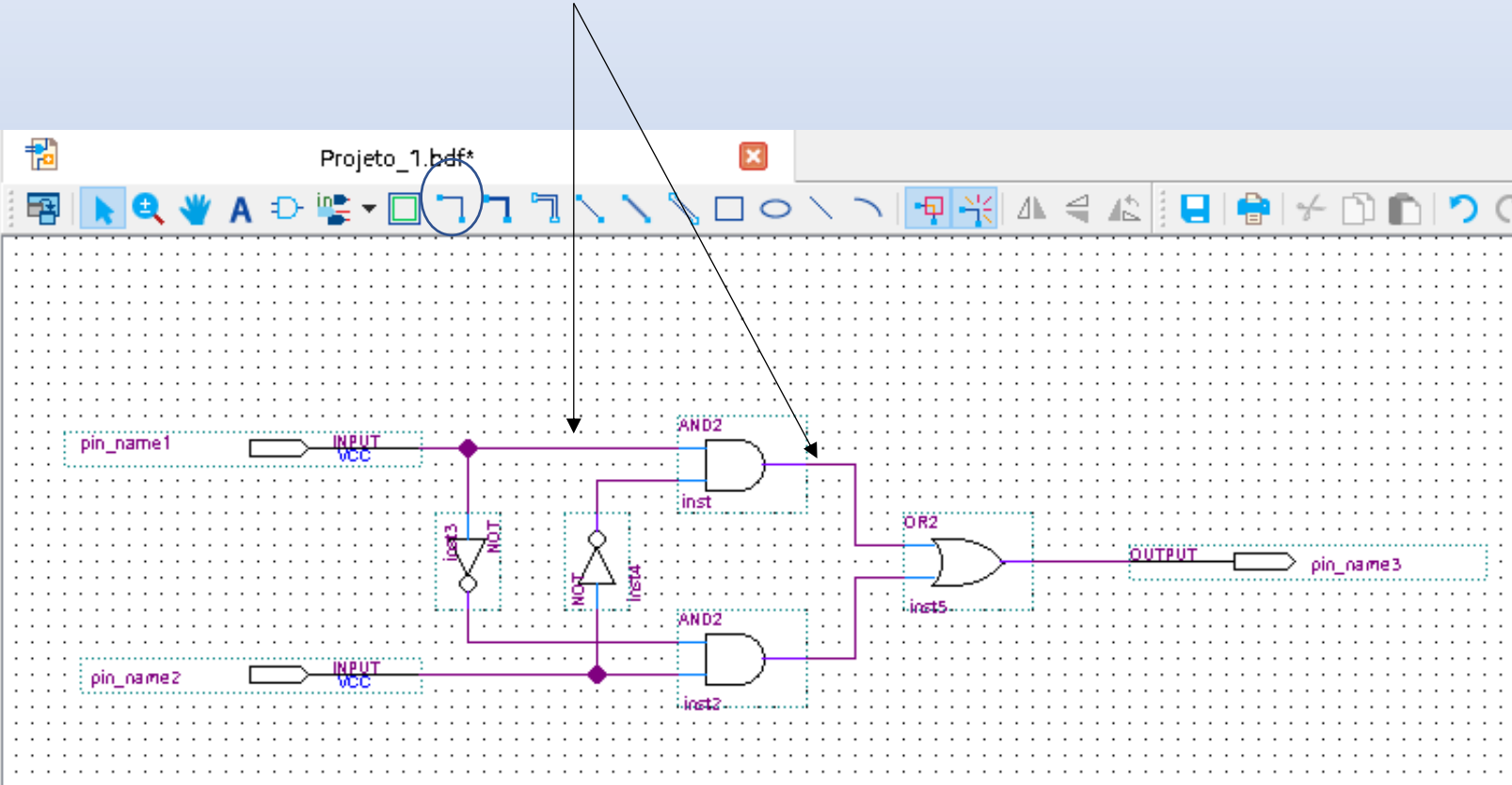
# SOFTWARE QUARTUS PRIME Lite Edition

Posicione o terminal de saida



# SOFTWARE QUARTUS PRIME Lite Edition

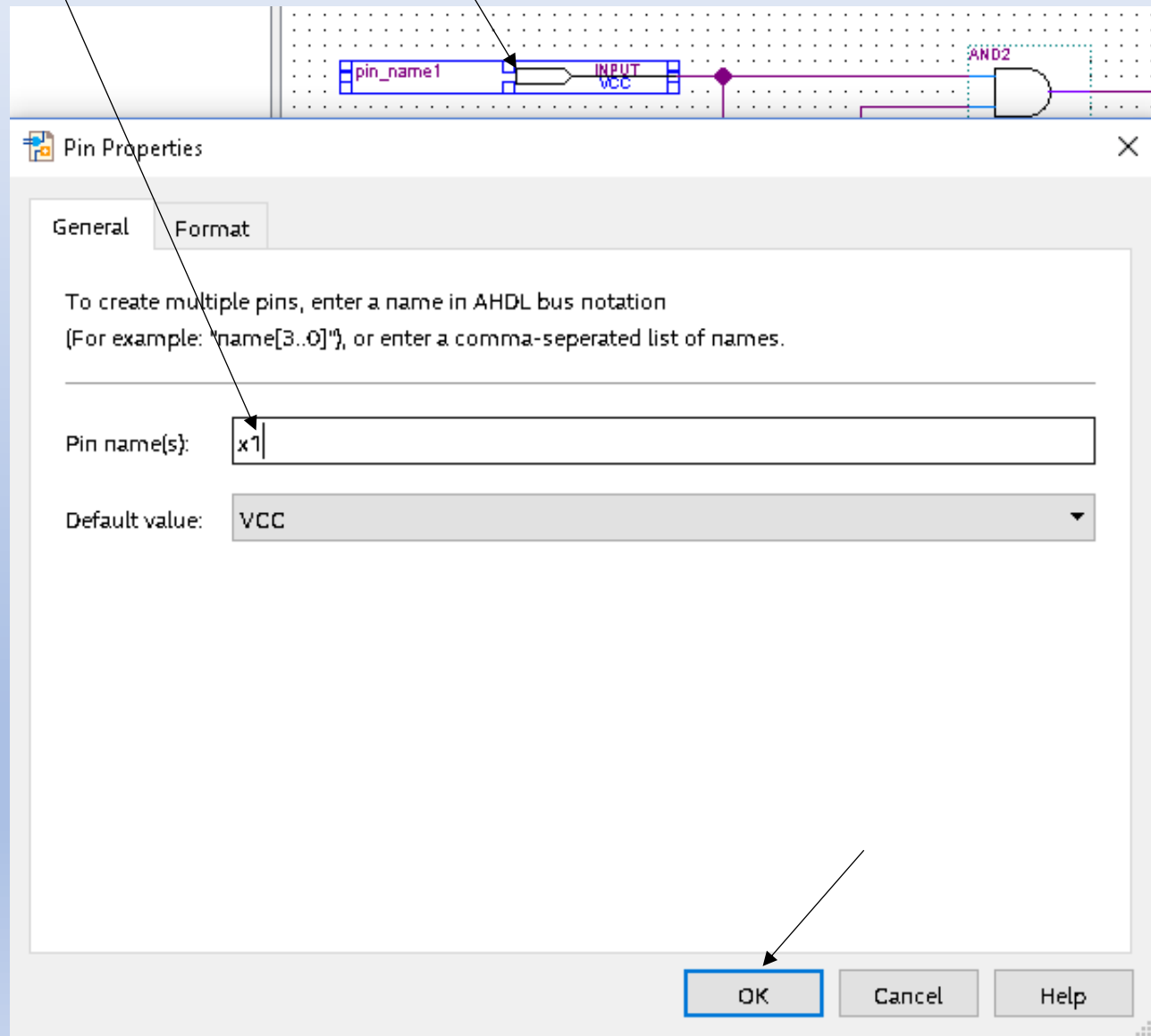
Interligação entre os componentes



# SOFTWARE QUARTUS PRIME Lite Edition

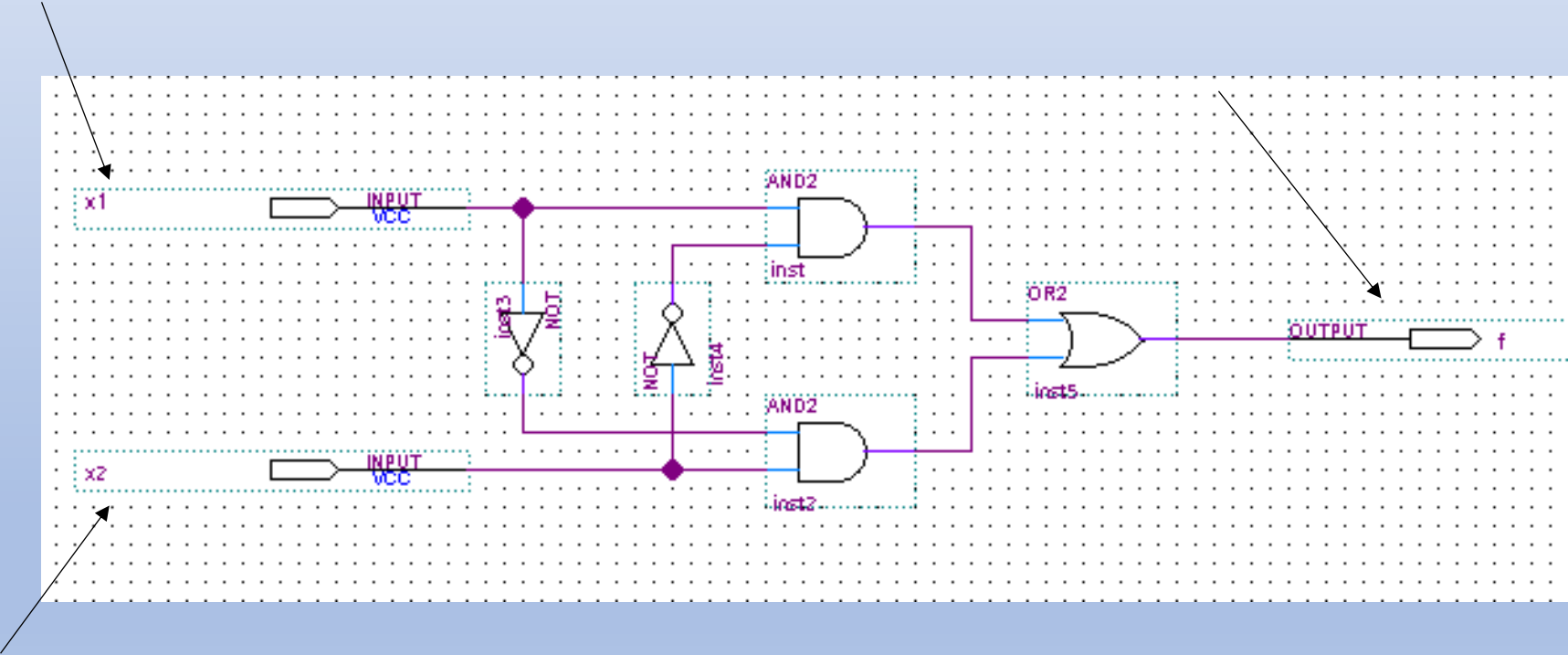
Atribuir nomes aos pinos de entrada e saída

Pin Name - duplo clique



# SOFTWARE QUARTUS PRIME Lite Edition

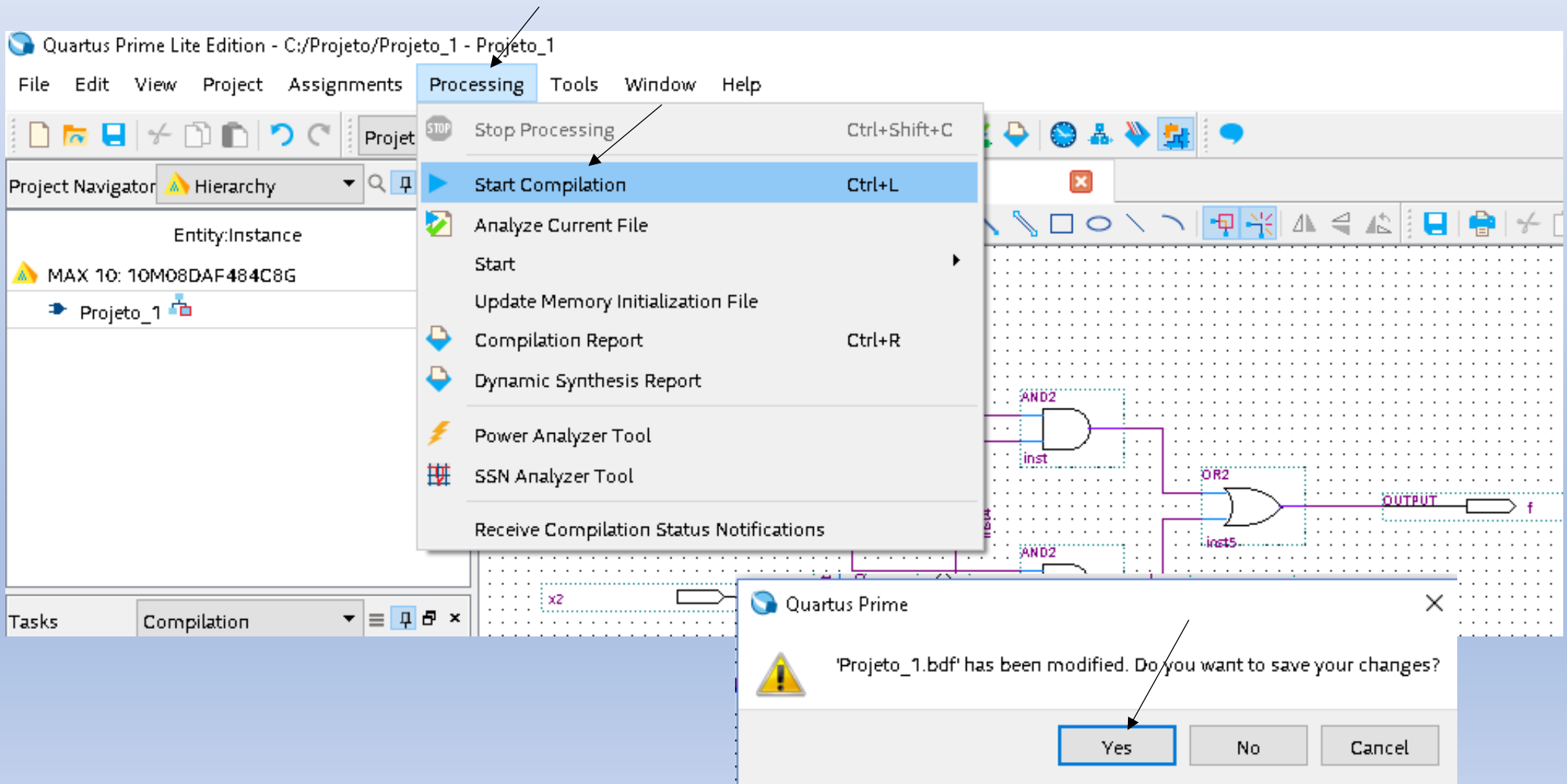
Atribuir nomes aos terminais



# SOFTWARE QUARTUS PRIME Lite Edition

## Compilação do Projeto

Processing - Start Compilation (O projeto deve ser salvo antes de compilar)



# SOFTWARE QUARTUS PRIME Lite Edition

## Etapas da compilação

## Resumo da compilação

The screenshot displays the Quartus Prime Lite Edition interface. The 'Tasks' window on the left shows the compilation process with green checkmarks for 'Compile Design', 'Analysis & Synthesis', 'Fitter (Place & Route)', 'Assembler (Generate programr', and 'Timing Analysis'. The 'Table of Contents' window in the center lists various reports, with 'Flow Summary' selected. The 'Flow Summary' window on the right provides a detailed overview of the compilation results.

Flow Status	Successful - Fri Aug 30 19:01:37 2019
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	Projeto_1
Top-level Entity Name	Projeto_1
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	2 / 49,760 (< 1 %)
Total registers	0
Total pins	3 / 360 (< 1 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

# SOFTWARE QUARTUS PRIME Lite Edition

## Etapas da compilação

The screenshot displays the compilation progress window in Quartus Prime. The 'Task' list on the left shows the following steps, all with green checkmarks indicating completion:

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Timing Analysis

The 'Timing Analyzer' window is active, showing resource usage statistics:

Resource	Used	Total	Percentage
Total virtual pins	0		
Total memory bits	0 / 387,072		{ 0 % }
Embedded Multiplier 9-bit elements	0 / 48		{ 0 % }
Total PLLs	0 / 2		{ 0 % }
UFM blocks	0 / 1		{ 0 % }
ADC blocks	0 / 1		{ 0 % }

The message window at the bottom shows a green message: "293000 Quartus Prime Full Compilation was successful. 0 errors, 13 warnings". An arrow points from the text "Indicacao ou Erros quando houver." below to the message window.

Indicacao ou Erros quando houver.



# SOFTWARE QUARTUS PRIME Lite Edition

Vincular os Pinos do FPGA as Entradas e Saidas do Pojeto

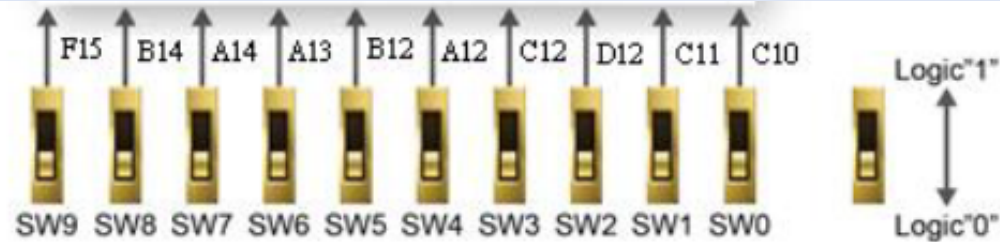


Figure 3-15 Connections between the slide switches and MAX 10 FPGA

Table 3-4 Pin Assignment of Slide Switches

Signal Name	FPGA Pin No.	Description	I/O Standard
SW0	PIN_C10	Slide Switch[0]	3.3-V LVTTTL
SW1	PIN_C11	Slide Switch[1]	3.3-V LVTTTL
SW2	PIN_D12	Slide Switch[2]	3.3-V LVTTTL
SW3	PIN_C12	Slide Switch[3]	3.3-V LVTTTL
SW4	PIN_A12	Slide Switch[4]	3.3-V LVTTTL
SW5	PIN_B12	Slide Switch[5]	3.3-V LVTTTL
SW6	PIN_A13	Slide Switch[6]	3.3-V LVTTTL
SW7	PIN_A14	Slide Switch[7]	3.3-V LVTTTL
SW8	PIN_B14	Slide Switch[8]	3.3-V LVTTTL
SW9	PIN_F15	Slide Switch[9]	3.3-V LVTTTL

# SOFTWARE QUARTUS PRIME Lite Edition

Vincular os Pinos do FPGA as Entradas e Saidas do Pojeto

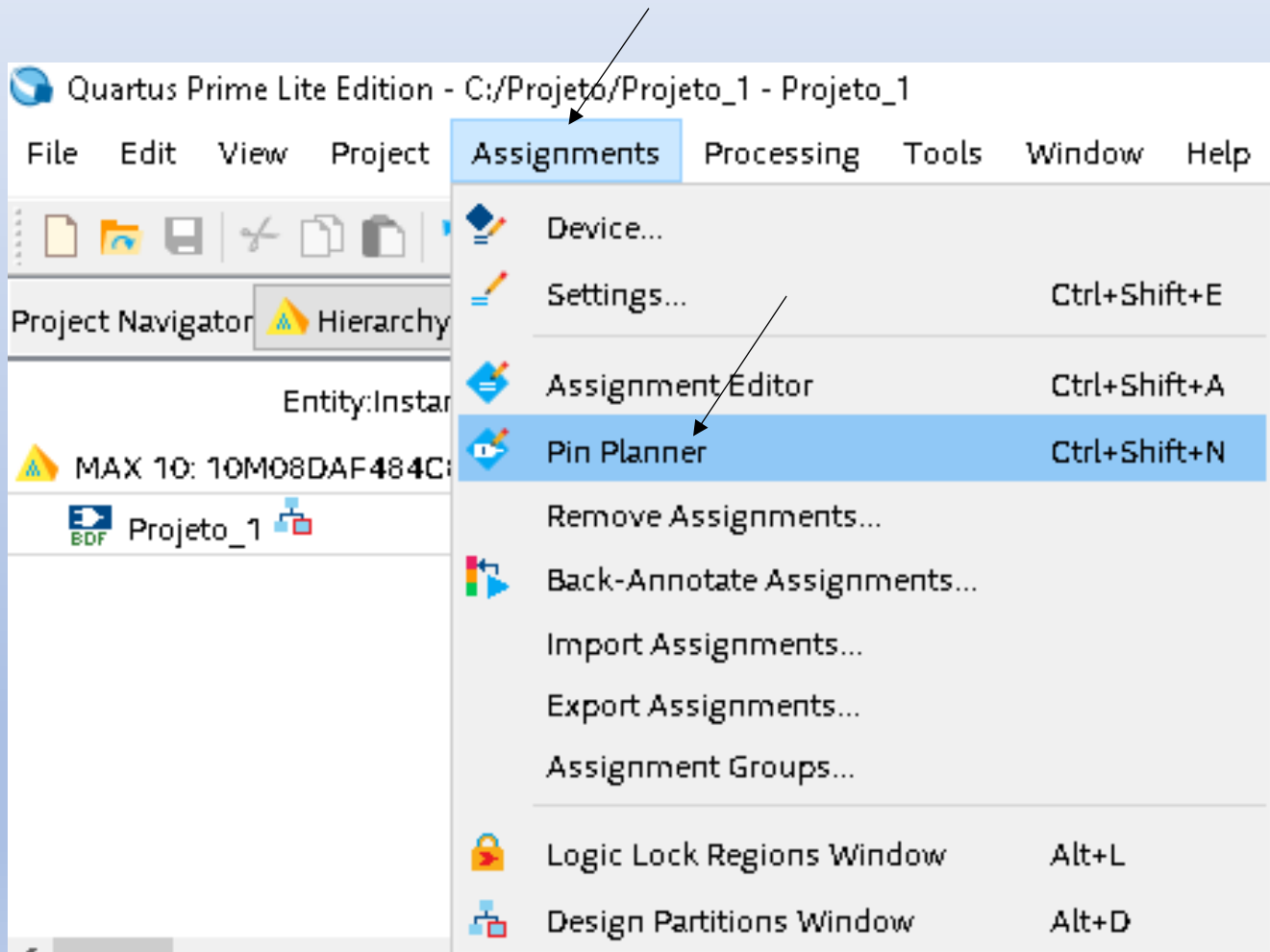
Table 3-5 Pin Assignment of LEDs

Signal Name	FPGA Pin No.	Description	I/O Standard
LEDR0	PIN_A8	LED [0]	3.3-V LVTTTL
LEDR1	PIN_A9	LED [1]	3.3-V LVTTTL
LEDR2	PIN_A10	LED [2]	3.3-V LVTTTL
LEDR3	PIN_B10	LED [3]	3.3-V LVTTTL
LEDR4	PIN_D13	LED [4]	3.3-V LVTTTL
LEDR5	PIN_C13	LED [5]	3.3-V LVTTTL
LEDR6	PIN_E14	LED [6]	3.3-V LVTTTL
LEDR7	PIN_D14	LED [7]	3.3-V LVTTTL
LEDR8	PIN_A11	LED [8]	3.3-V LVTTTL
LEDR9	PIN_B11	LED [9]	3.3-V LVTTTL

# SOFTWARE QUARTUS PRIME Lite Edition

Vincular os Pinos do FPGA as Entradas e Saidas do Pojeto

Assignments – Pin Planner



# SOFTWARE QUARTUS PRIME Lite Edition

F – PIN\_A8, x1 – PIN\_C10 e PIN\_C11

The screenshot displays the Quartus Prime Lite Edition interface for pin assignment. The central window shows the "Top View- Wire Band" for the device "MAX 10 - 10M50DAF484C7G". The pin assignment table at the bottom is as follows:

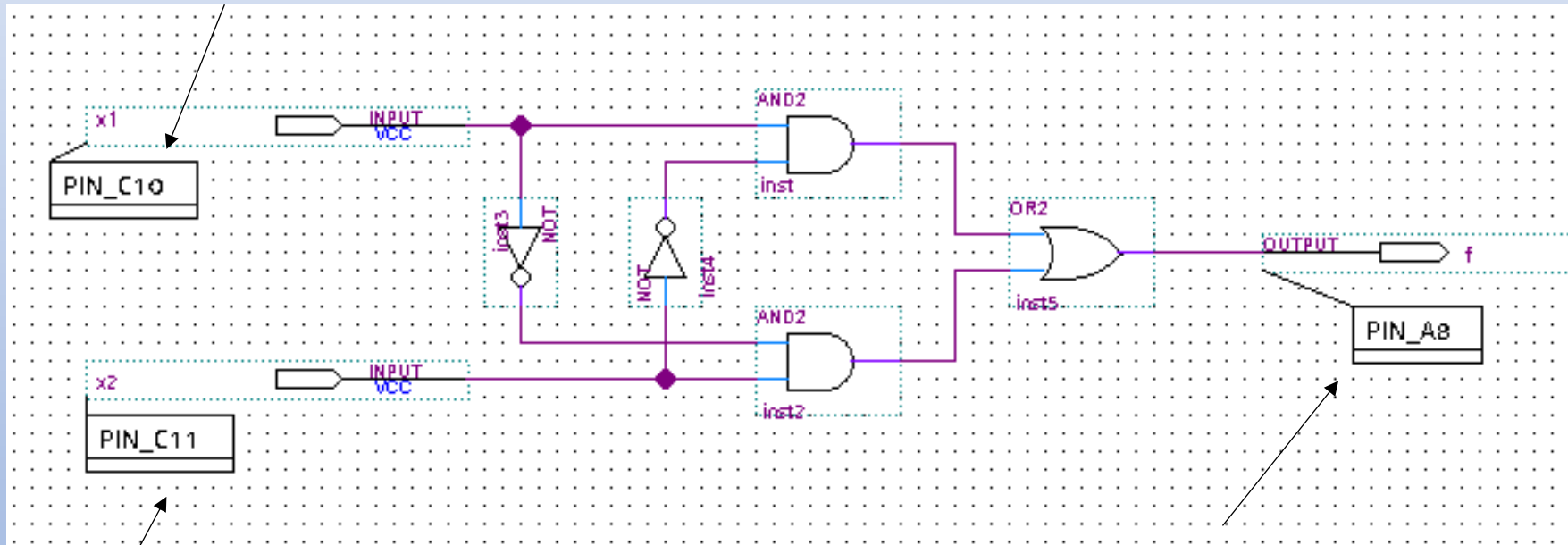
Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
out f	Output	pin_A8	7	B7_NO	PIN_W8	2.5 V (default)
in x1	Input	PIN_C10	7	B7_NO	PIN_AB4	2.5 V (default)
in x2	Input	PIN_C11	7	B7_NO	PIN_AA3	2.5 V (default)
<<new node>>						

The Pin Legend on the right lists various pin types and their symbols, including DIFF\_n, DIFF\_p, DQ, DQS, DQSB, CLK\_n, CLK\_p, Other PLL, Other dual purp..., TDI, TCK, TMS, TDO, VREF, VCCP/VCCR/V..., and VCCA.

# SOFTWARE QUARTUS PRIME Lite Edition

Compilar o Projeto novamente

Processing – Start Compilation

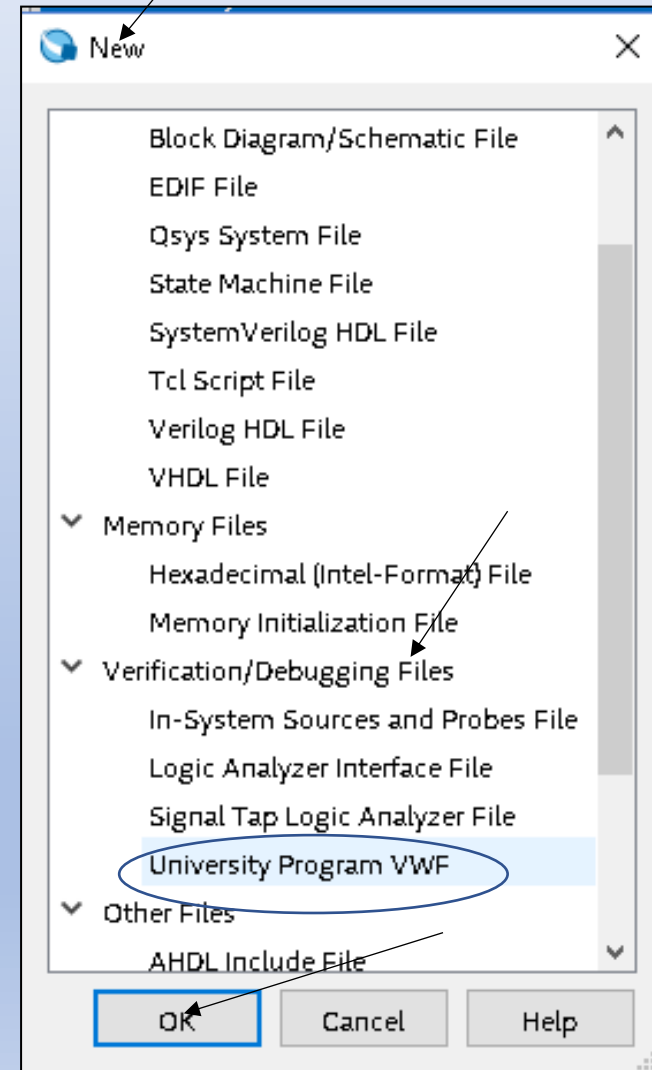


# SOFTWARE QUARTUS PRIME Lite Edition

Simulacao Funcional do Circuito

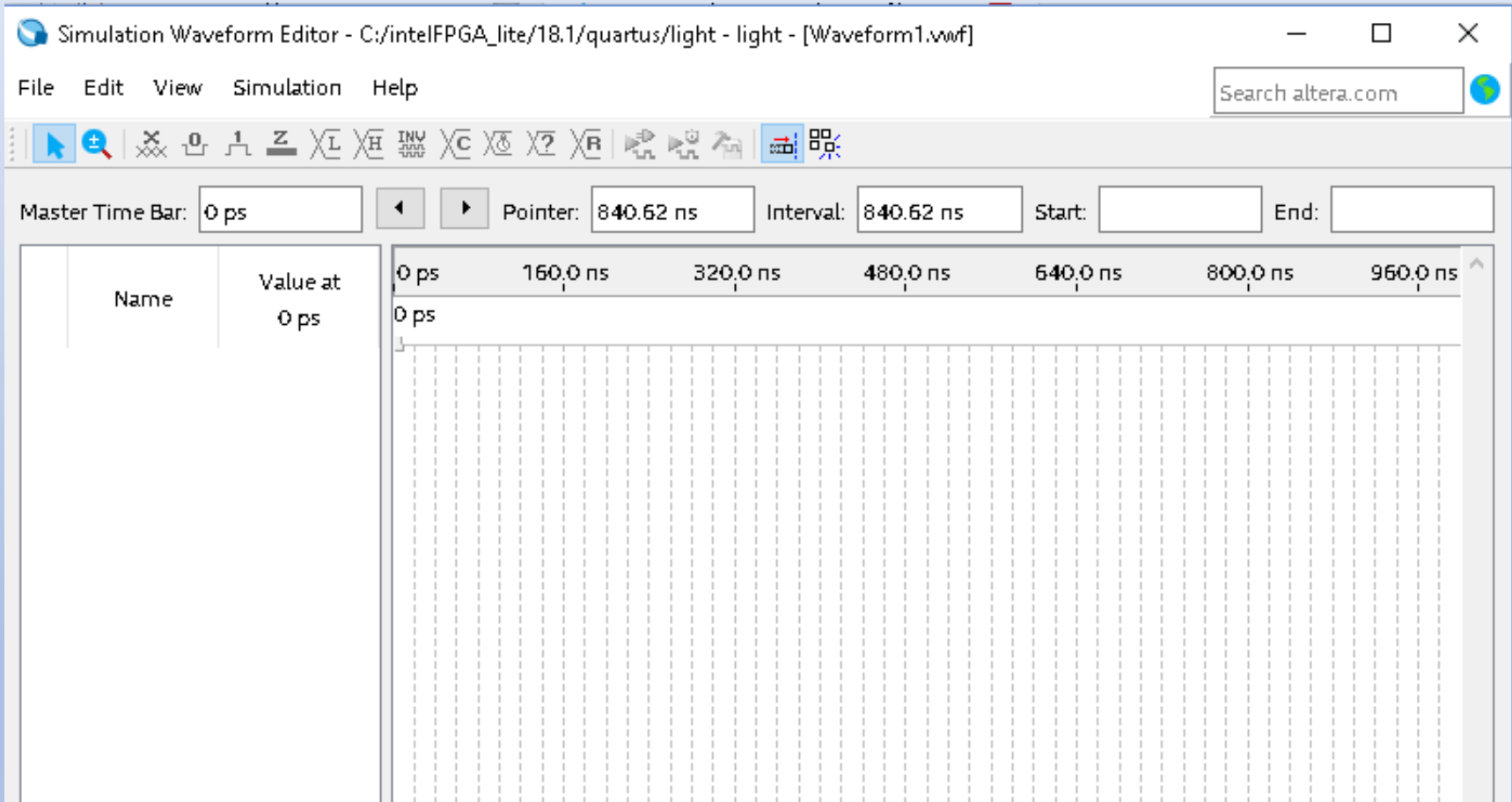
Criacao dos Vetores de Testes – Formas de Onda

File – New – Verification/Debugging Files –  
University Program VWF



# SOFTWARE QUARTUS PRIME Lite Edition

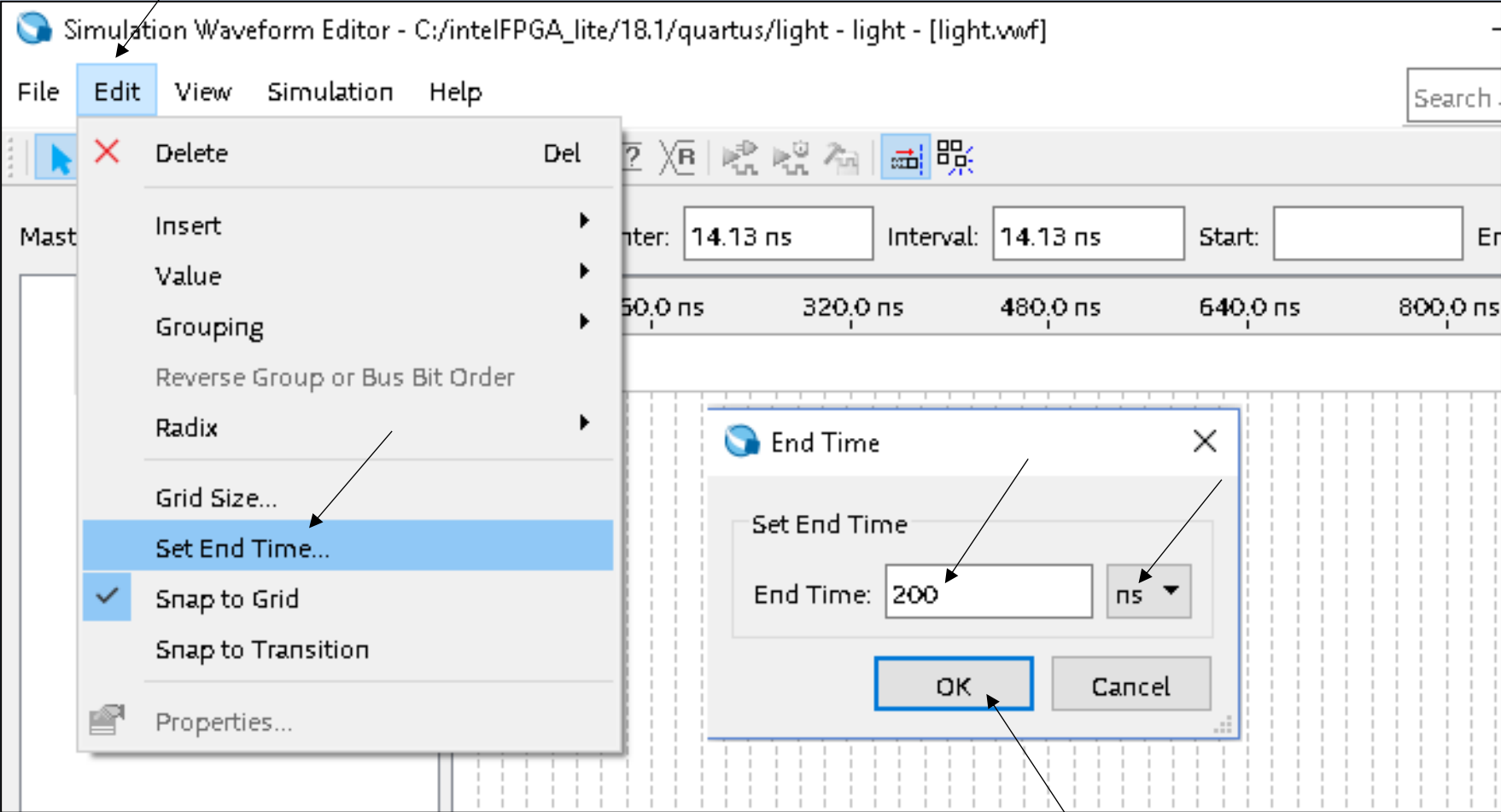
## Tela do Editor de Forma de Ondas



# SOFTWARE QUARTUS PRIME Lite Edition

Configure o tempo de Simulacao de 0 a 200 ns

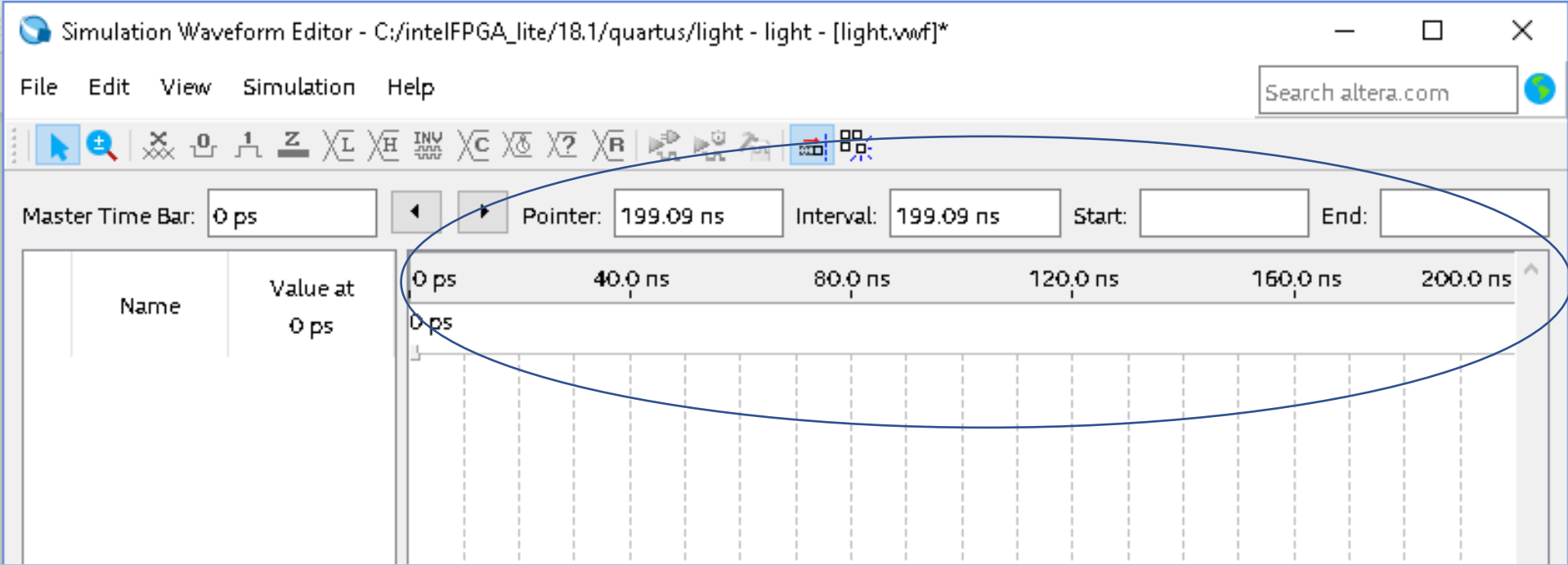
Edit – Set End Time





# SOFTWARE QUARTUS PRIME Lite Edition

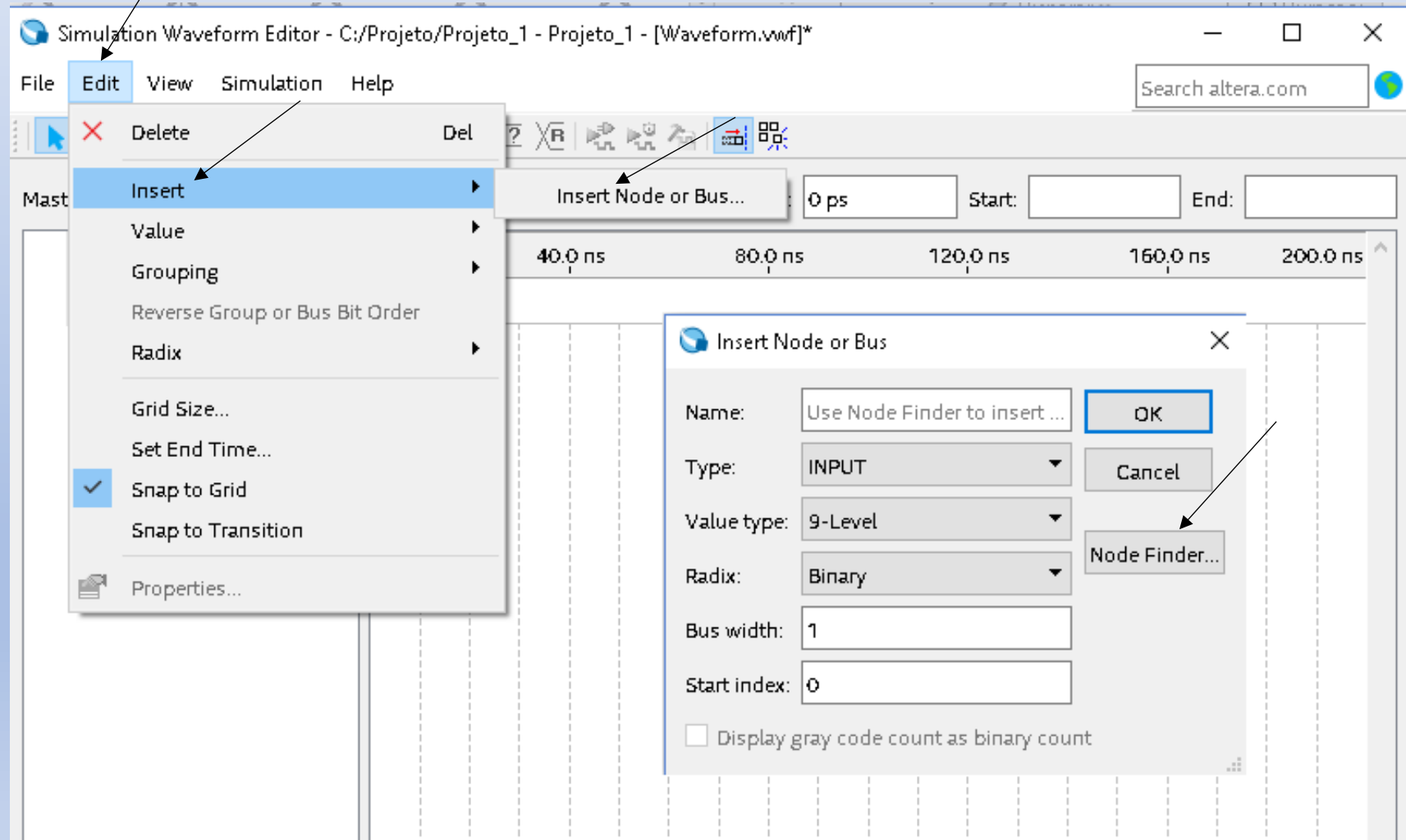
Editor de Forma de Ondas



# SOFTWARE QUARTUS PRIME Lite Edition

Incluir as entradas e saídas no Editor de Forma de Ondas

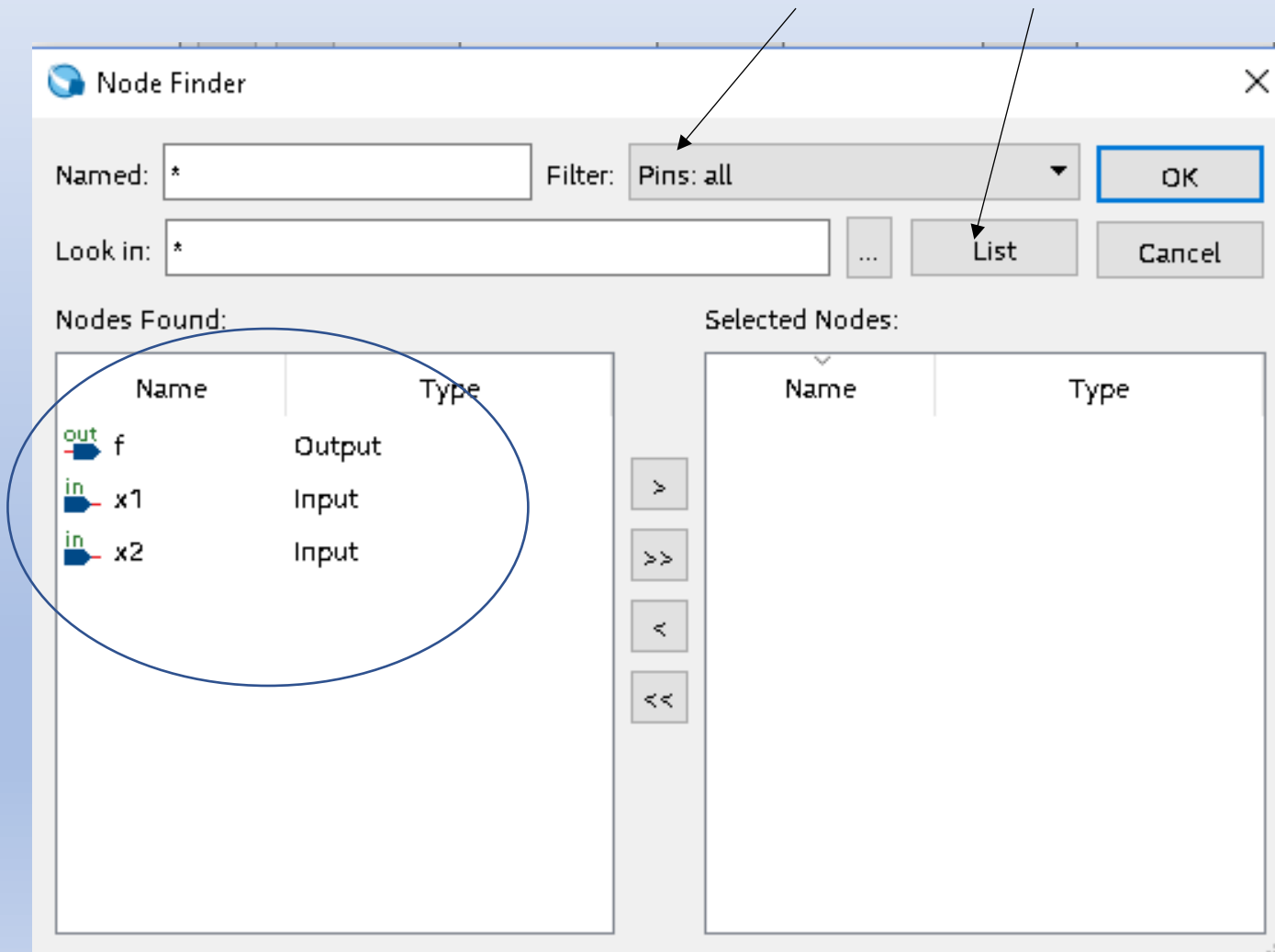
Edit – Insert – Inset Node or Bus – Node Finder



# SOFTWARE QUARTUS PRIME Lite Edition

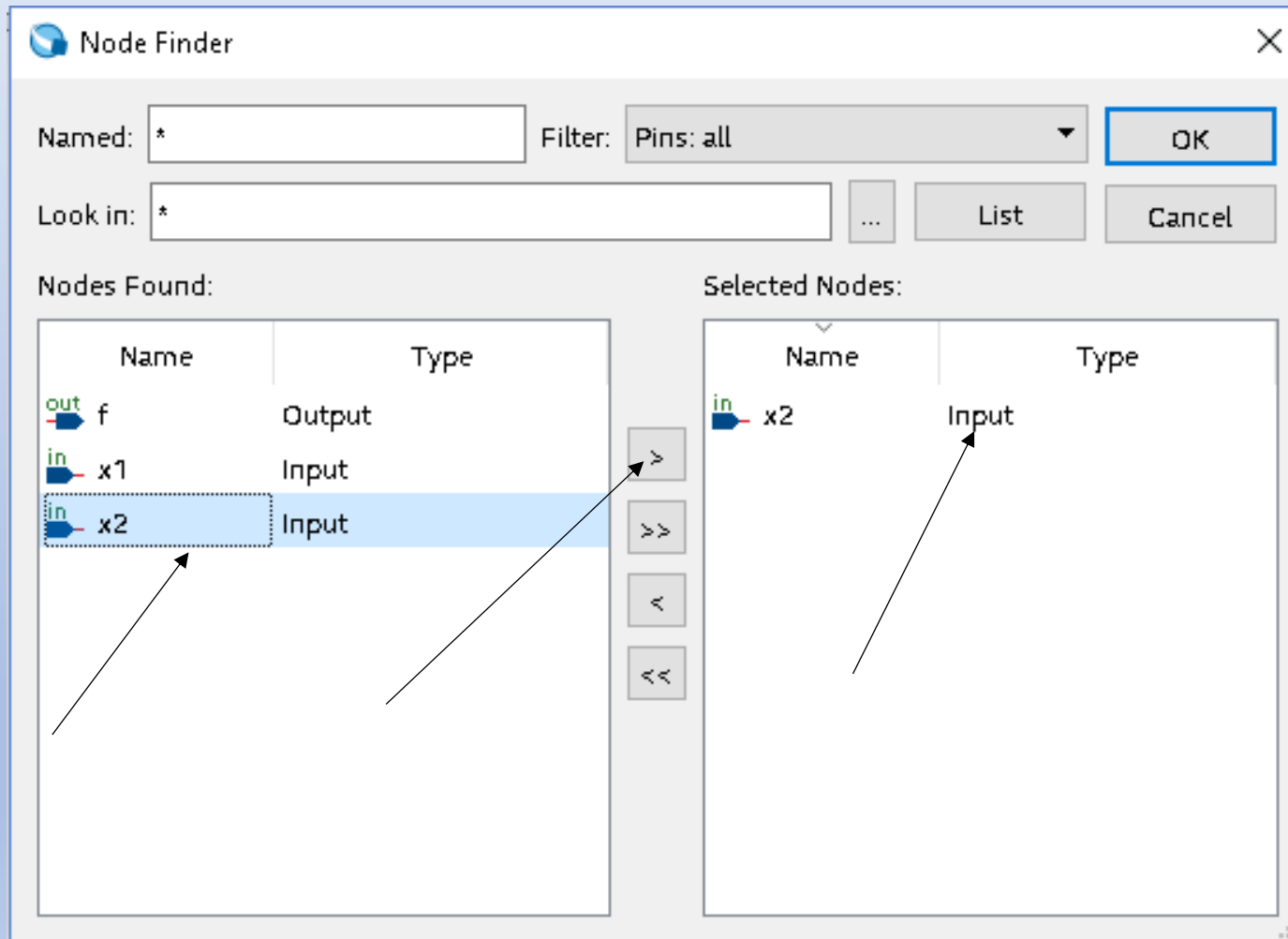
Indicacao das Entradas e Saidas

Pins: all - List



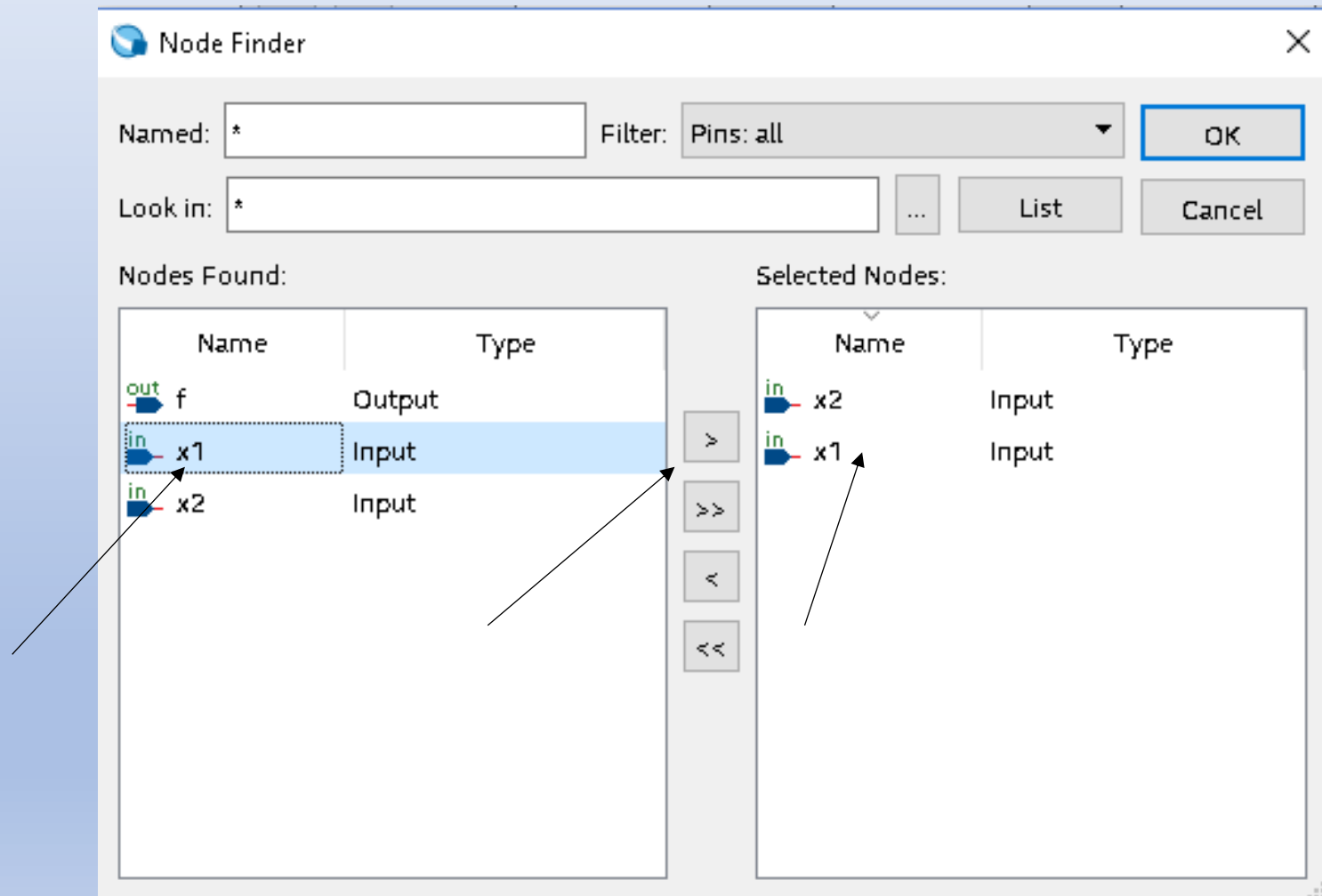
# SOFTWARE QUARTUS PRIME Lite Edition

Selecionando a entrada x2 para Simulacao



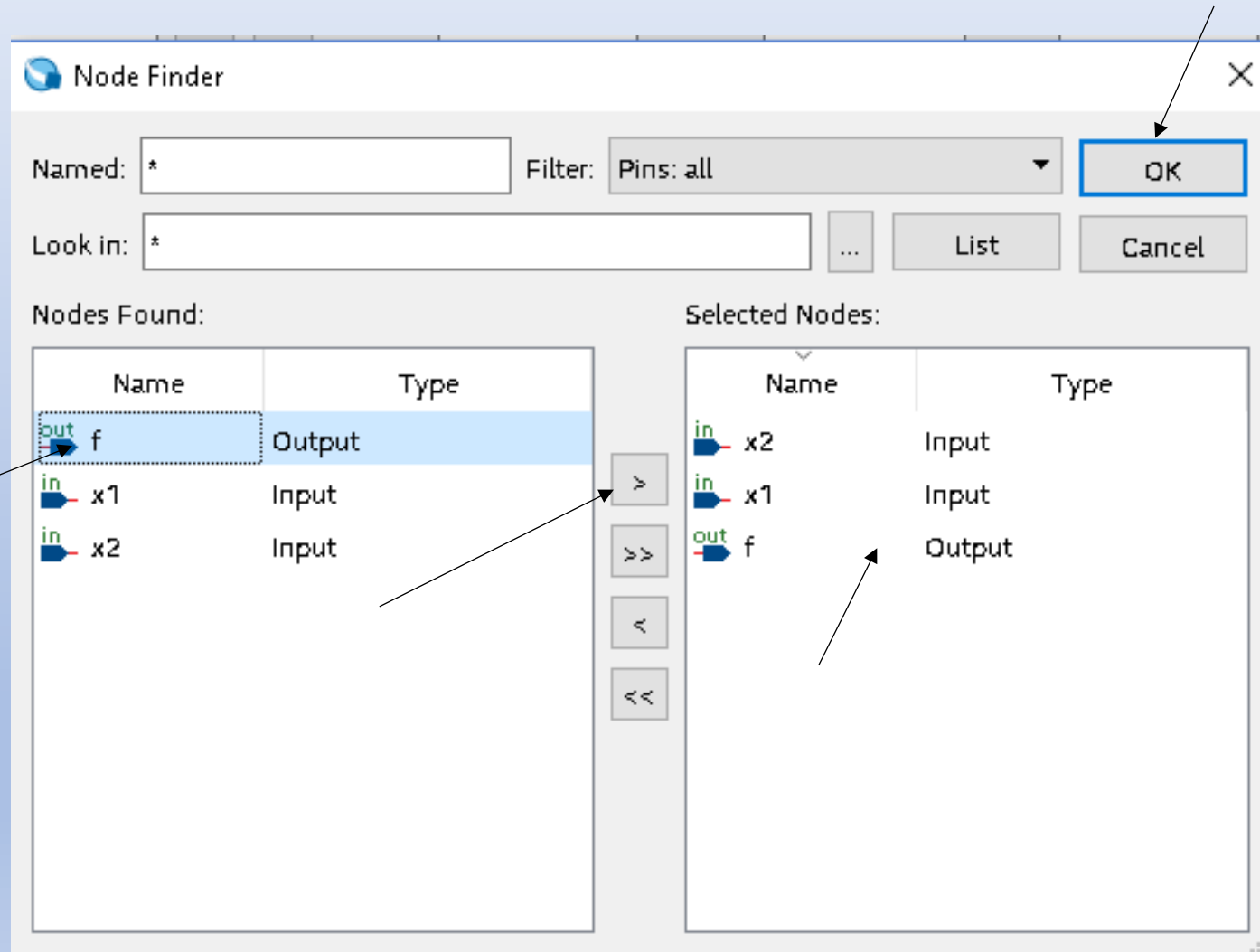
# SOFTWARE QUARTUS PRIME Lite Edition

Selecionando a entrada x1 para Simulacao



# SOFTWARE QUARTUS PRIME Lite Edition

Selecionando a saída f para Simulação



# SOFTWARE QUARTUS PRIME Lite Edition

**Insert Node or Bus** [X]

Name:

Type:  ▼

Value type:  ▼

Radix:  ▼

Bus width:

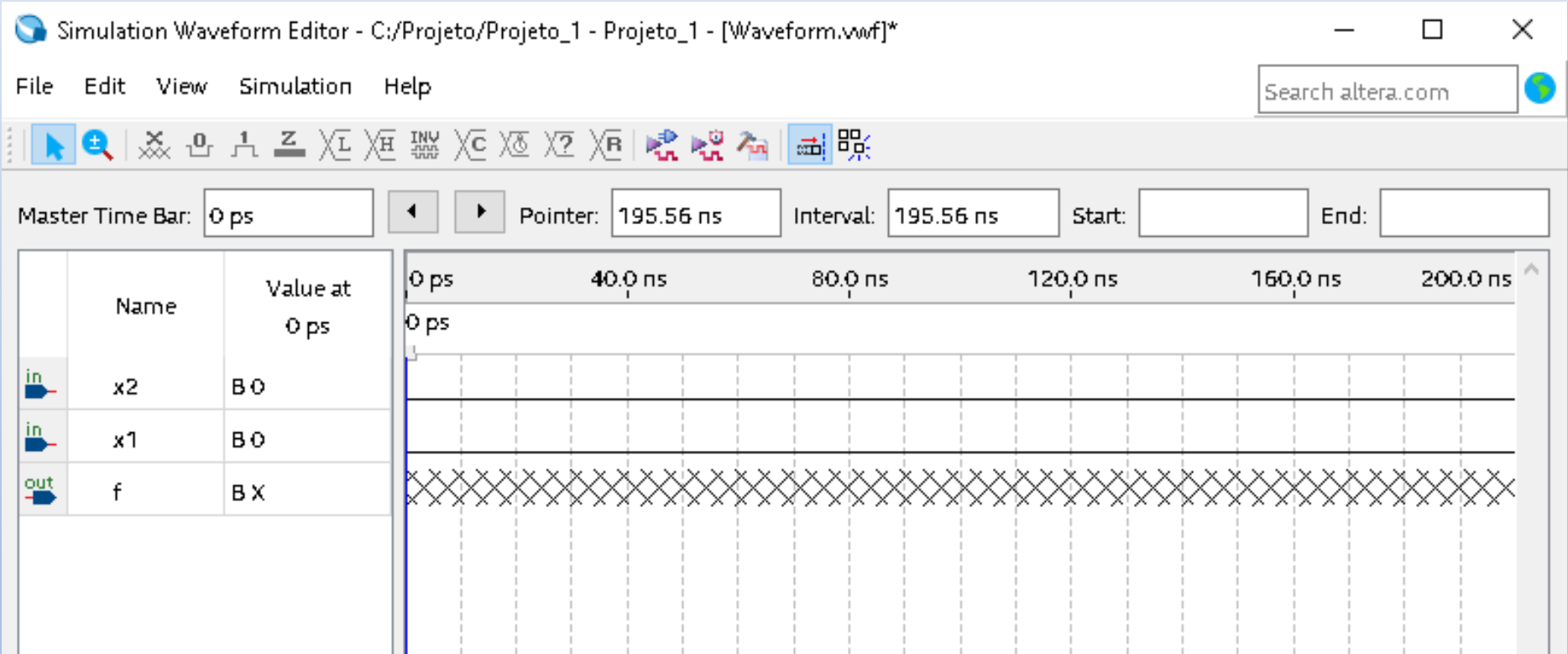
Start index:

Display gray code count as binary count

Buttons: OK, Cancel, Node Finder...

# SOFTWARE QUARTUS PRIME Lite Edition

## Entradas e Saidas no Editor de Formas de Ondas





# SOFTWARE QUARTUS PRIME Lite Edition

Selecione a Entrada x2 - Sinal de OverwriterClock

The screenshot shows the Simulation Waveform Editor interface. The main window title is "Simulation Waveform Editor - C:/Projeto/Projeto\_1 - Projeto\_1 - [Waveform.wwf]\*". The menu bar includes File, Edit, View, Simulation, and Help. The toolbar contains various icons for waveform manipulation. The Master Time Bar shows 0 ps, and the Pointer is at 199.09 ns. The Interval is 199.09 ns, Start is 0 ps, and End is 200.0 ns. The waveform display shows three signals: x2 (input), x1 (input), and f (output). The signal x2 is highlighted in blue. A "Clock" dialog box is open, showing the configuration for the selected signal. The dialog has a title bar with the Quartus logo and a close button. The main area is titled "Base waveform on time period" and contains three input fields: "Period:" with a value of 50.0 ns, "Offset:" with a value of 0.0 ns, and "Duty cycle (%):" with a value of 50. The "OK" button is highlighted with a blue border, and an arrow points to it from the bottom of the image.

Name	Value at 0 ps
x2	B 0
x1	B 0
f	B X

Base waveform on time period

Period: 50.0 ns

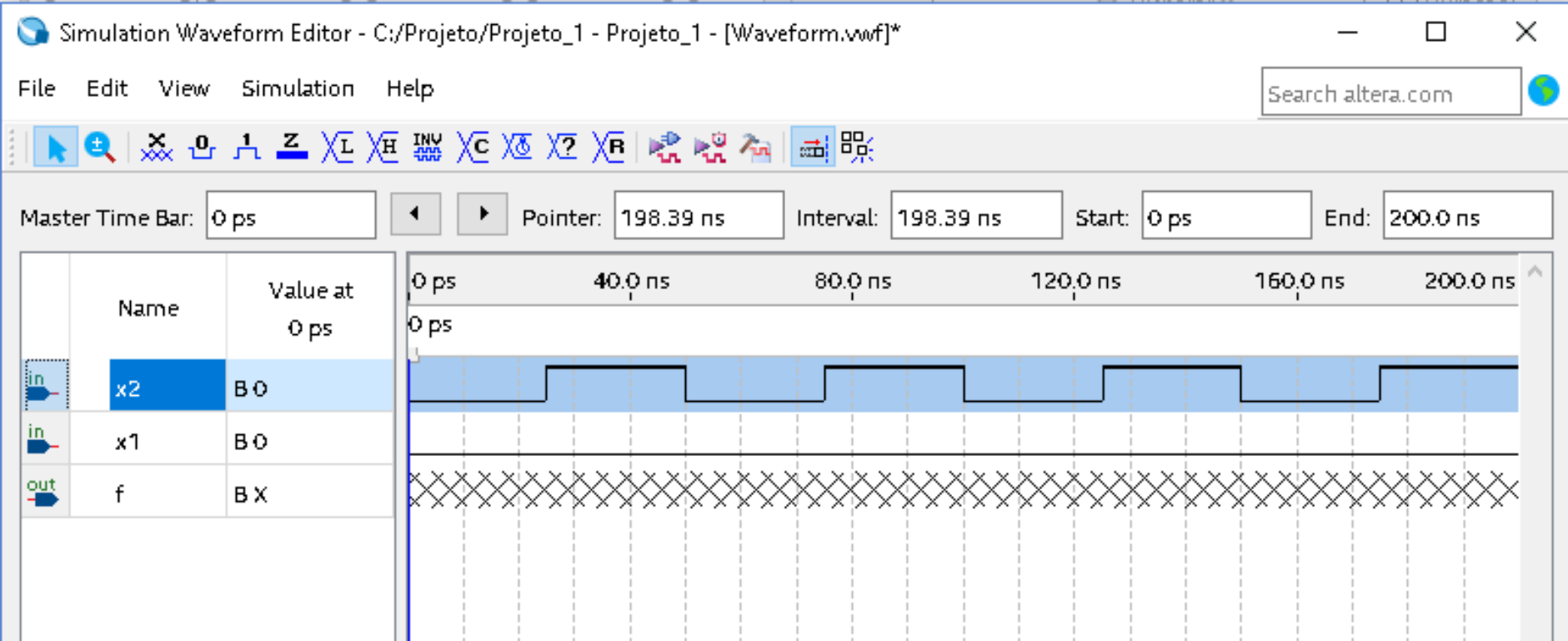
Offset: 0.0 ns

Duty cycle (%): 50

OK Cancel

# SOFTWARE QUARTUS PRIME Lite Edition

Selecione a Entrada x2 - Sinal de Clock C



# SOFTWARE QUARTUS PRIME Lite Edition

Selecione a Entrada x1 - Sinal de OverwriterClock

The screenshot shows the Simulation Waveform Editor interface. The main window displays a waveform for three signals: 'x2' (input), 'x1' (input), and 'f' (output). The 'x1' signal is highlighted in blue. A 'Clock' dialog box is open, showing the configuration for the selected signal. The dialog has the following fields:

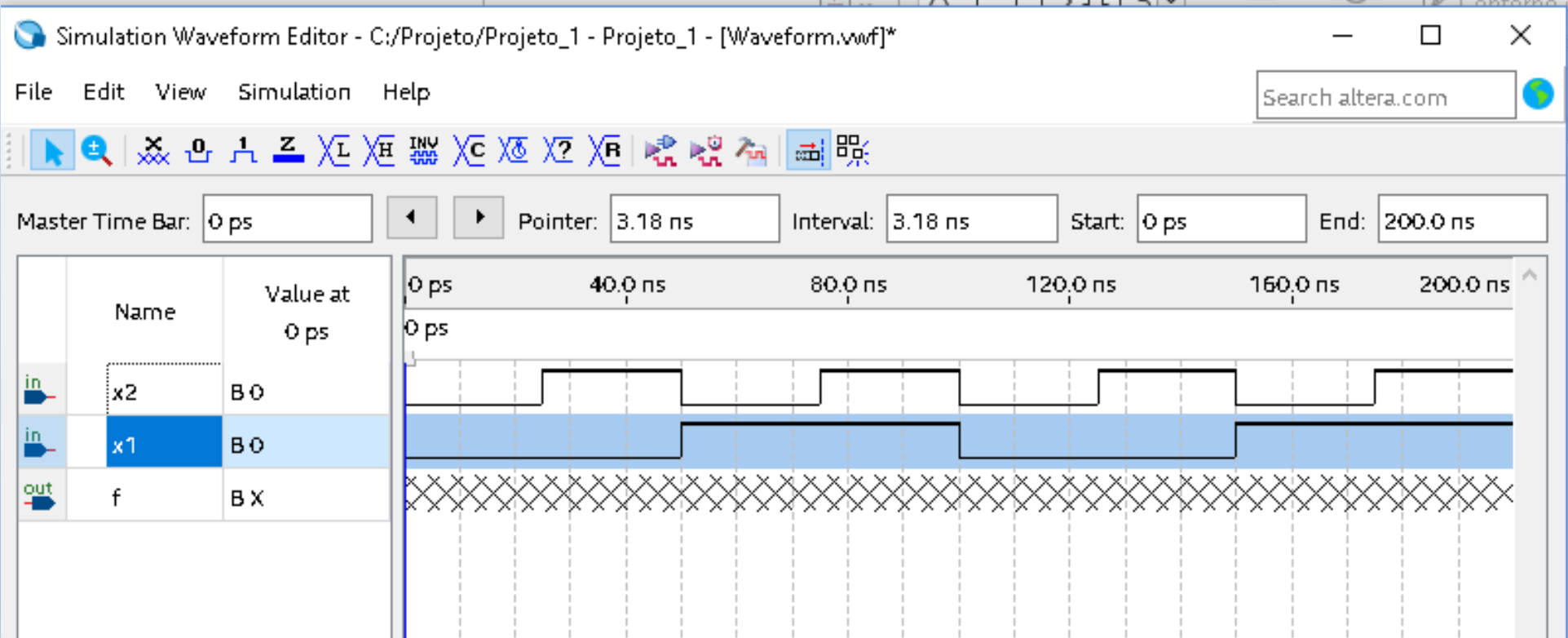
- Base waveform on time period
- Period: 100.0 ns
- Offset: 0.0 ns
- Duty cycle (%): 50
- Buttons: OK, Cancel

The 'OK' button is highlighted with a blue border. The waveform editor shows a time scale from 0 ps to 200.0 ns with major ticks every 40.0 ns. The 'x1' signal is a square wave with a period of 100 ns and a 50% duty cycle.

# SOFTWARE QUARTUS PRIME Lite Edition

Selecione a Entrada x1 - Sinal de OverwriterClock

Salvar o Projeto\_1 no diretorio C:/Projeto



# SOFTWARE QUARTUS PRIME Lite Edition

Simulation Options

**Caution: Improperly modifying these settings can cause the simulation to fail**

HDL Language:  Verilog  VHDL (The language used for the testbench and netlist)

Functional Simulation Settings | Timing Simulation Settings

Testbench Generation Command (Functional Simulation):  
`quartus_eda --gen_testbench --tool=modelsim_oem --format=verilog --write_settings_files=off Projeto_1 -c F`

Netlist Generation Command (Functional Simulation):  
`quartus_eda --write_settings_files=off --simulation --functional=on --flatten_buses=off --tool=modelsim_oem`

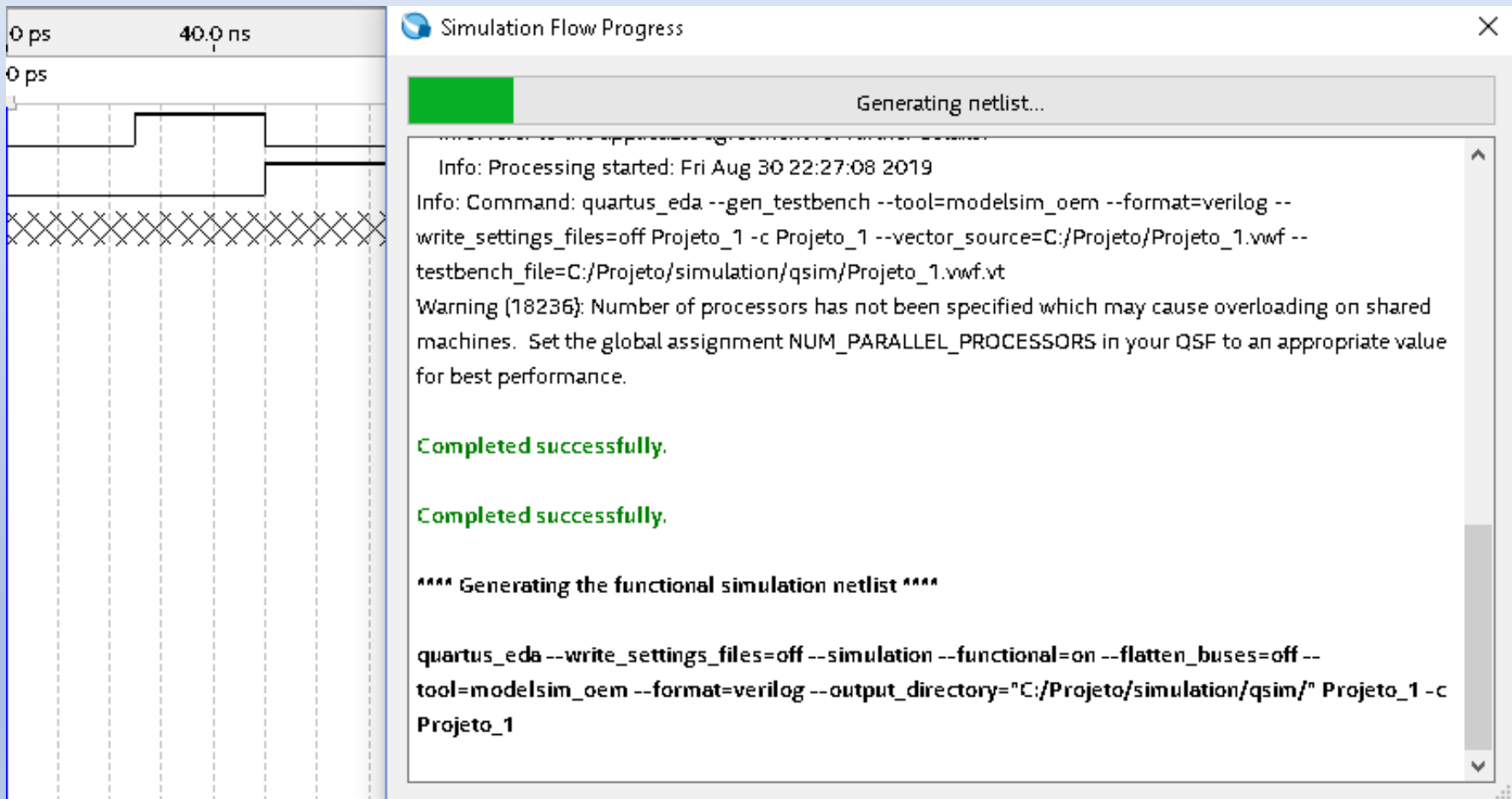
ModelSim Script (Functional Simulation):  

```
onerror {exit -code 1}
vlib work
vlog -work work Projeto_1.vo
vlog -work work Projeto_1.vwf.vt
vsim -novopt -c -t 1ps -L fiftyfivenm_ver -L altera_ver -L altera_mf_ver -L 220model_ver -L sgate_ver -L altera_
vcd file -direction Projeto_1.msim.vcd
vcd add -internal Projeto_1_vlg_vec_tst/*
vcd add -internal Projeto_1_vlg_vec_tst/i1/*
proc simTimestamp {} {
  echo "Simulation time: $::now ps"
  if { [string equal running [runStatus]] } {
    after 2500 simTimestamp
  }
}
```

Restore Defaults | **Save** | Cancel

# SOFTWARE QUARTUS PRIME Lite Edition

## Tool - Run Functional Simulation



The image shows a screenshot of the Quartus Prime software interface. On the left, a timing diagram is visible, showing a signal transition from 0 ps to 40.0 ns. The signal is high for a period and then drops to low. Below the signal, there is a pattern of 'X' marks, likely representing a simulation error or a specific data point.

On the right, a "Simulation Flow Progress" window is open, showing the progress of the simulation. The progress bar is green, indicating that the simulation is complete. The window title is "Simulation Flow Progress" and the progress bar label is "Generating netlist...".

The progress window contains the following text:

```
Info: Processing started: Fri Aug 30 22:27:08 2019
Info: Command: quartus_eda --gen_testbench --tool=modelsim_oem --format=verilog --
write_settings_files=off Projeto_1 -c Projeto_1 --vector_source=C:/Projeto/Projeto_1.vwf --
testbench_file=C:/Projeto/simulation/qsim/Projeto_1.vwf.vt
Warning [18236]: Number of processors has not been specified which may cause overloading on shared
machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value
for best performance.

Completed successfully.

Completed successfully.

**** Generating the functional simulation netlist ****

quartus_eda --write_settings_files=off --simulation --functional=on --flatten_buses=off --
tool=modelsim_oem --format=verilog --output_directory="C:/Projeto/simulation/qsim/" Projeto_1 -c
Projeto_1
```

# SOFTWARE QUARTUS PRIME Lite Edition

The screenshot shows the 'Options' dialog box in Quartus Prime Lite Edition. The 'Tools' menu is open, and 'Options...' is selected. The 'EDA Tool Options' category is selected in the left sidebar. The 'General' sub-category is expanded, and the 'EDA Tool Options' section is highlighted. The 'ModelSim' entry in the table is highlighted with a red box, and a red arrow points from it to a callout box.

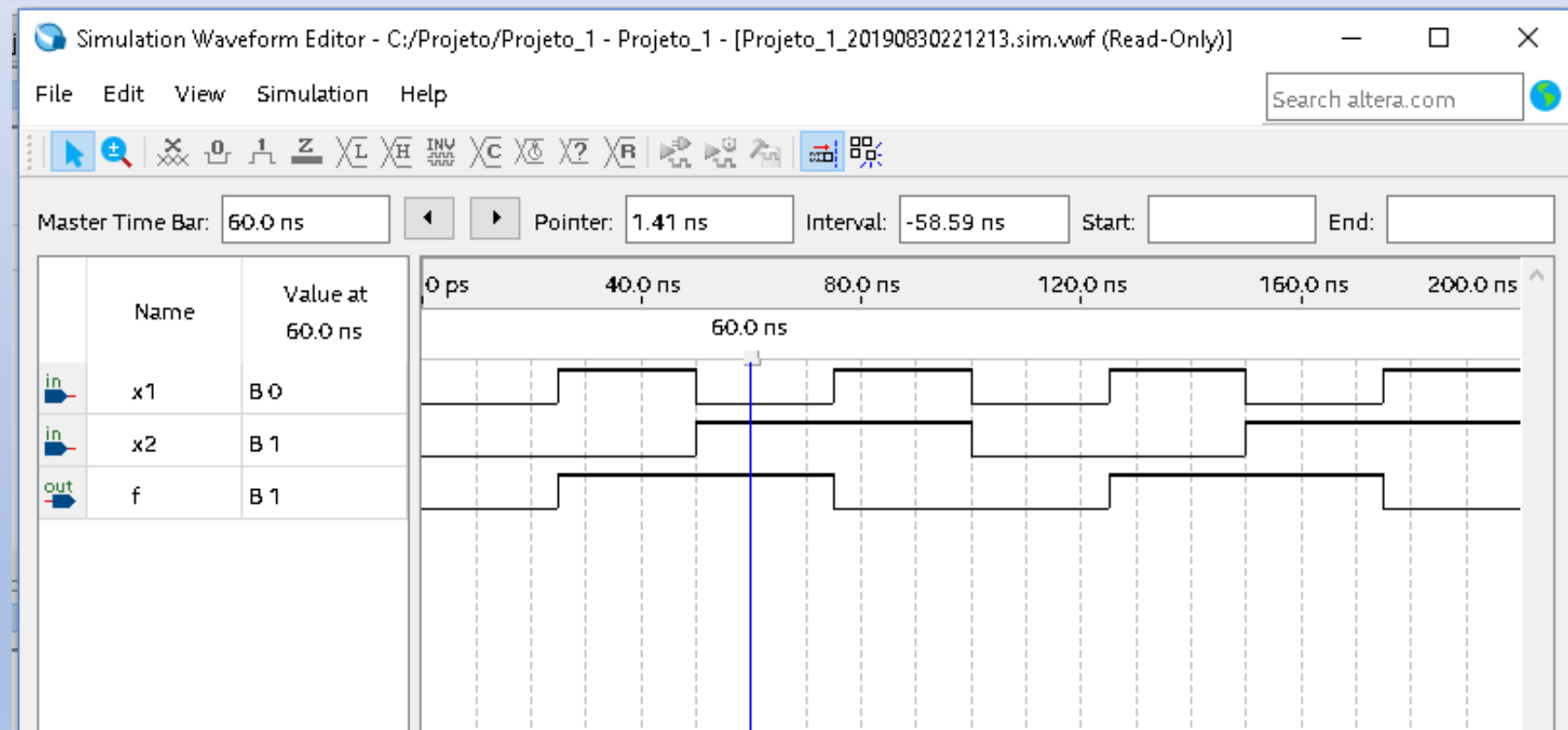
EDA Tool	Directory Containing Tool Executable
Precision S...	
Synplify	
Synplify Pro	
Active-HDL	
Riviera-PRO	
ModelSim	C:\intelFPGA_lite\17.1\modelsim_ase\win32aloem
QuestaSim	
ModelSim-...	

Caso apareça um erro na simulação solicitando o caminho do "ModelSim", volte ao Quartus e procure o caminho como indicado na figura... **OBS: Substitua o "17.1" pela versão do Quartus instalado.**

# SOFTWARE QUARTUS PRIME Lite Edition

Salvar o Projeto\_1 no diretorio C:/Projeto

Simulation – Run Functional Simulation



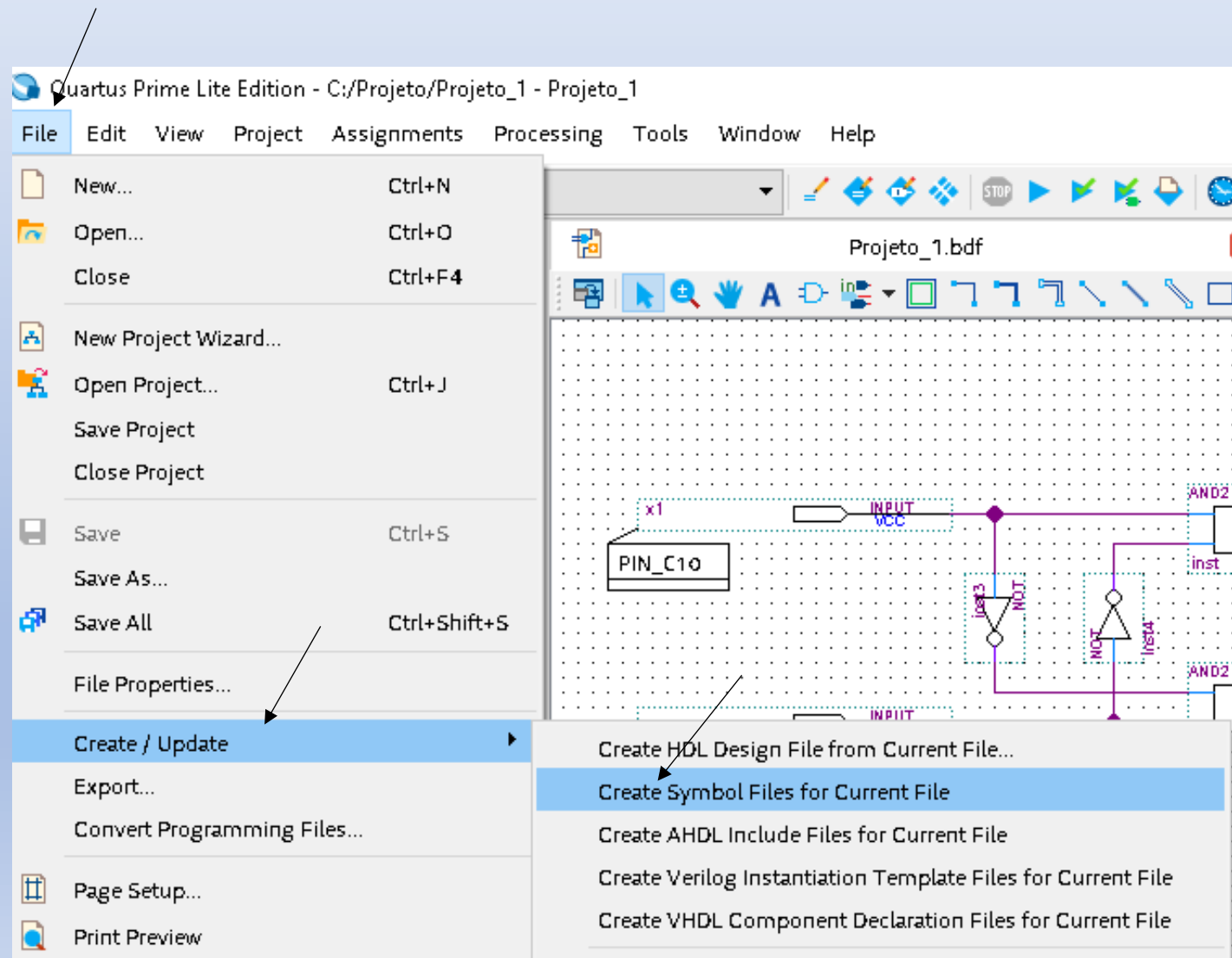


# SOFTWARE QUARTUS PRIME Lite Edition

Criar um Simbolo Grafico

Na Tela do Editor Grafico :

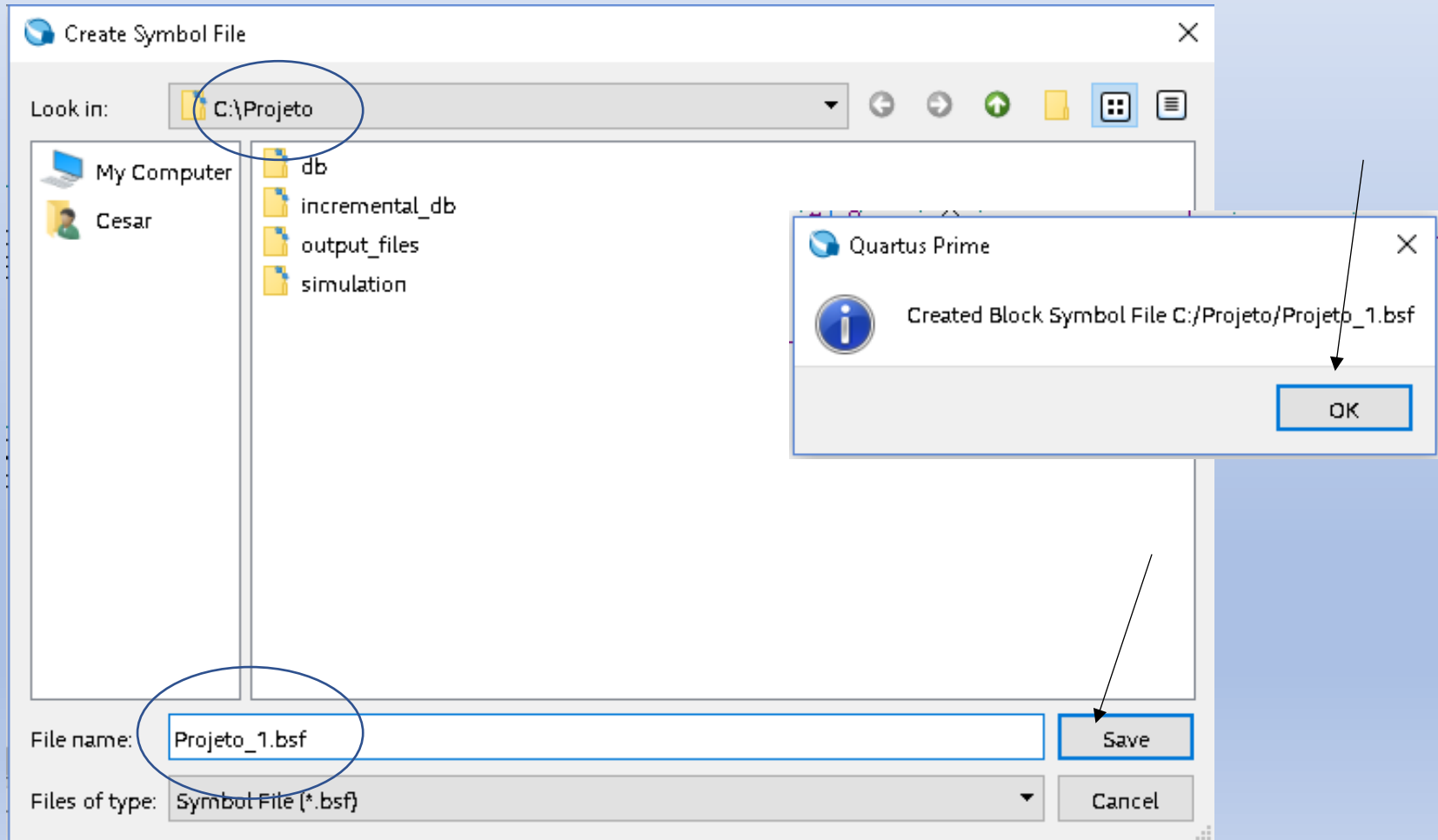
File – Create/Update – Create Symbol Files for Current File



# SOFTWARE QUARTUS PRIME Lite Edition

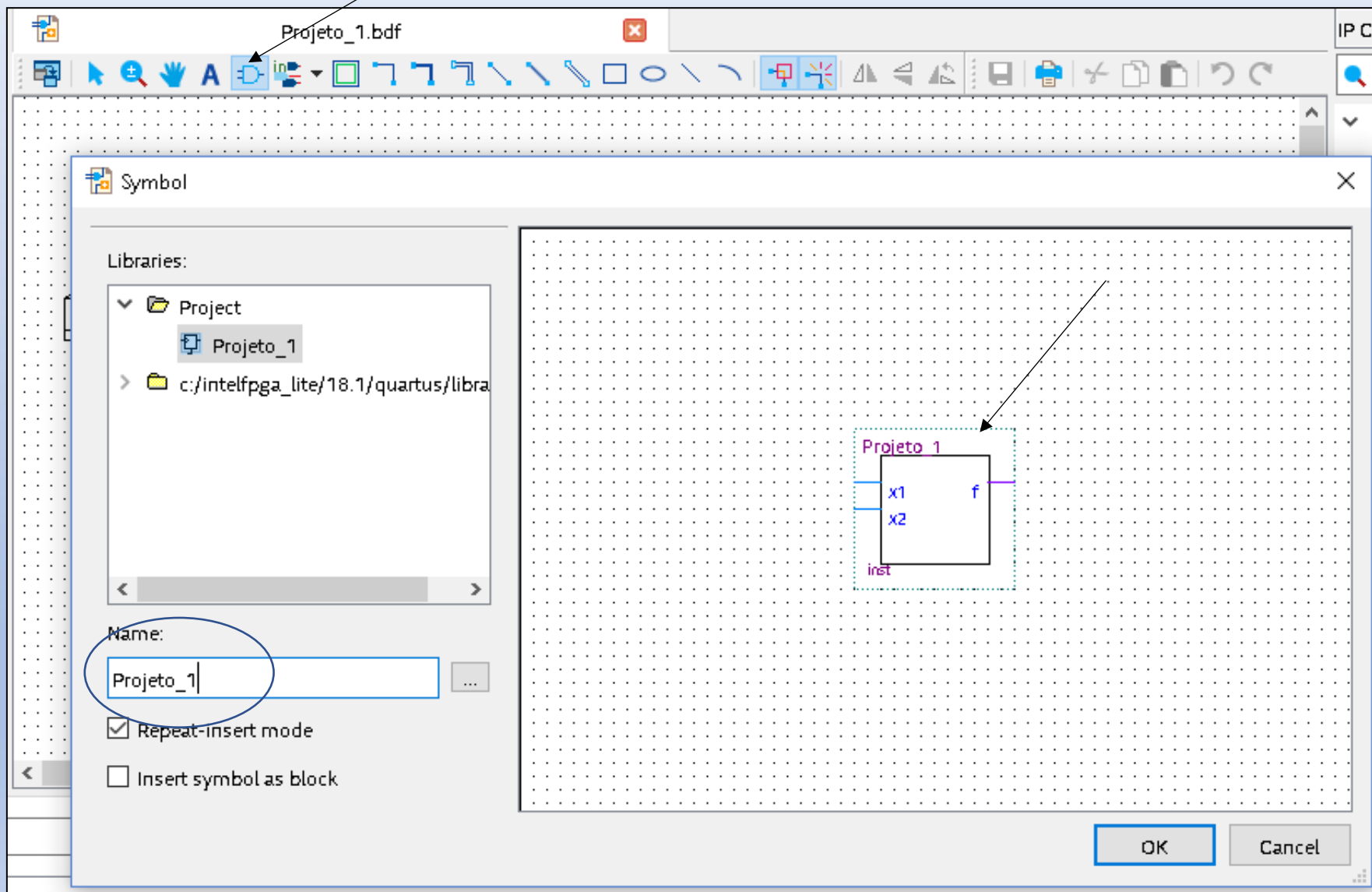
Criar um Simbolo Grafico

Salve o Arquivo - Ok



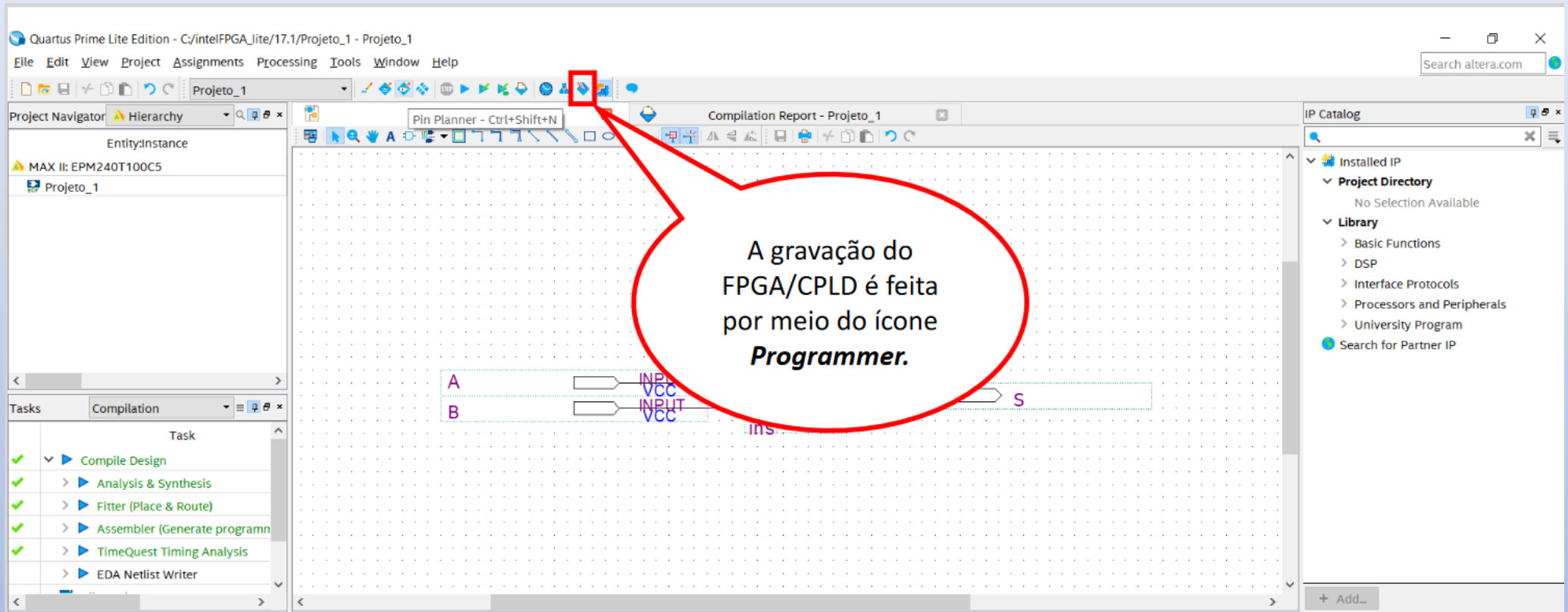
# SOFTWARE QUARTUS PRIME Lite Edition

## Seleção o Simbolo Grafico Criado



# Descarregar o programa no Kit do FPGA

## Menu – Tools - Programmer



# Descarregar o programa no Kit do FPGA

## Menu – Tools - Programmer

The image shows three sequential screenshots of the Altera Programmer software interface, illustrating the process of programming an FPGA device. Red circles and arrows highlight key steps and elements.

**Hardware Selection:** The first screenshot shows the 'Hardware Setup...' dialog box. The 'Available hardware items' table lists 'USB-Blaster' as the selected hardware. A red circle highlights the 'USB-Blaster' entry.

Hardware	Server	Port
USB-Blaster	Local	USB-0

**Programming Options:** The second screenshot shows the main Programmer window. The 'Hardware Setup...' dropdown is set to 'USB-Blaster [USB-0]'. The 'Start' button is highlighted with a red circle. The 'Program/Configure' checkbox is checked, and the 'Start' button is highlighted with a red circle.

**Successful Completion:** The third screenshot shows the 'Progress' bar at '100% (Successful)'. The 'Start' button is highlighted with a red circle.

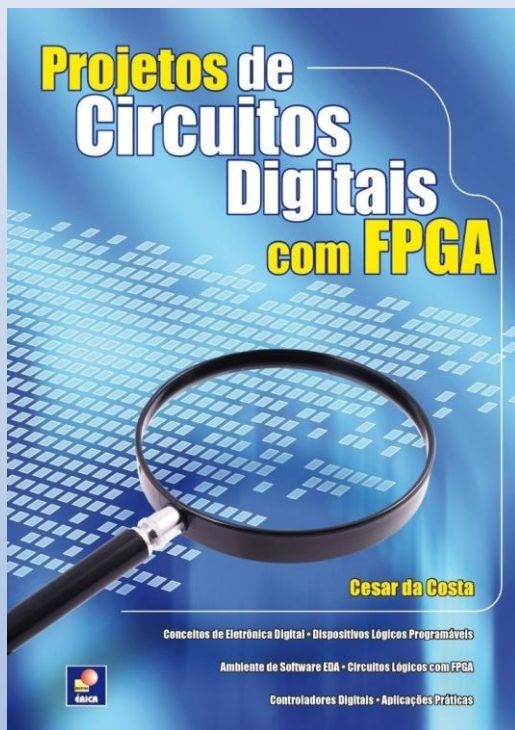
**Annotations:**

- A red circle highlights the 'Hardware Setup...' button in the top left of the first screenshot.
- A red circle highlights the 'USB-Blaster' entry in the 'Available hardware items' table.
- A red circle highlights the 'Start' button in the second screenshot.
- A red circle highlights the 'Program/Configure' checkbox in the second screenshot.
- A red circle highlights the 'Start' button in the third screenshot.
- A red circle highlights the 'Progress: 100% (Successful)' bar in the third screenshot.

**Text Annotations:**

- A red oval contains the text: "Selecione as caixas de seleção **Program/Configure** e clique em **Start**. A barra de progresso indicará quando o processo de gravação for finalizado."
- A red cloud contains the text: "Caso o Hardware não tenha sido identificado automaticamente, esta opção deve ser selecionada. O gravador utilizado é o **USB-Blaster**."

# Conclusões



## Referência

<https://www.youtube.com/watch?v=a2zQPHc4D9k>

<https://www.youtube.com/watch?v=X2QuGO-mrEY>

Site [www.professorcesarcosta.com.br](http://www.professorcesarcosta.com.br)

### Tópicos:

- Disciplinas Ministradas T8LLC/LALOG;
- Kits Didáticos com FPGA;
- Clube do FPGA;
- FPGA;

Site [www.fpgacentral.com](http://www.fpgacentral.com)